UBM
Electronics

May 2012
www.tmworld.com

Test & MEASUREMENT WORLD®

THE MAGAZINE FOR QUALITY IN ELECTRONICS

SIGNAL INTEGRITY

Avoid a common S-parameter problem

24

RF PRODUCTION TEST

Improve production test of high-speed RF components

28

AVIONICS TEST

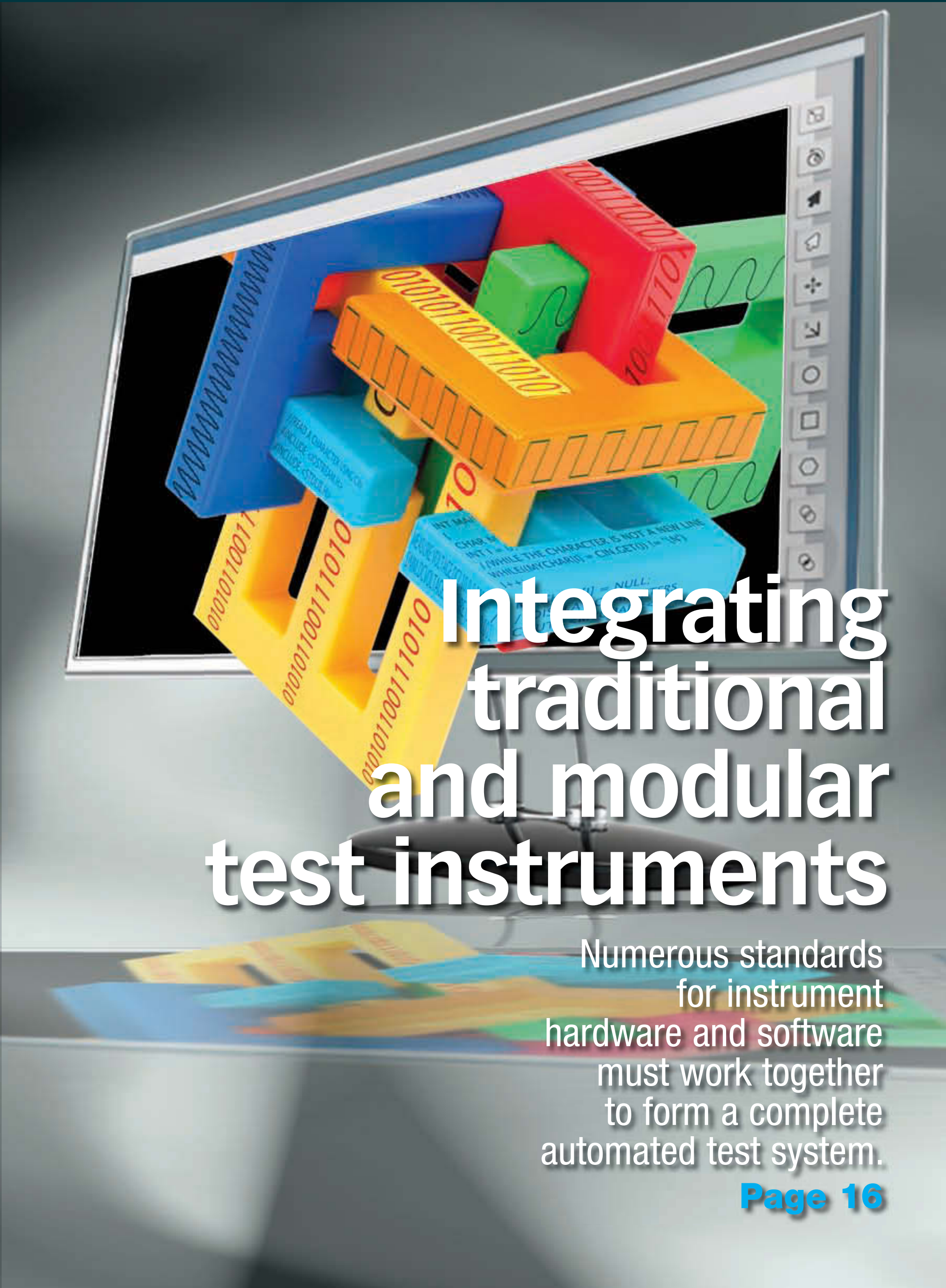
Testing aircraft AFDX systems

34

WAFER PROBING

High-temperature effects on wafer probing

14



Integrating traditional and modular test instruments

Numerous standards for instrument hardware and software must work together to form a complete automated test system.

Page 16


Agilent 34972A DAQ
Main
Monitor
Scan
34972A Connection Status
Connected: 192.168.10.102
34972A Operation Status
Ready
Monitor
Channel
Measurement
Mode
110
111
112
113
114
TC
Ther
RTD
B-type
E-type
J-type
K-type
N-type
Agilent 34972A
LXI Data Acquisition / Switch Unit
27.9
°C
101
LXI
Agilent 34901A
Agilent 34903A
Agilent 34907A
Agilent 34905A
Agilent 34904A
Agilent 34908A
Agilent 34902A
Agilent 34906A

Test & Measurement Equipment

High Performance Multi-Function I/O USB Data Acquisition Modules

- 16 Differential or 32 Single-Ended Analog Inputs, Expandable to 32 Differential/ 64 Single-Ended Channels
- 24-Bit Resolution
- Thermocouple or Voltage Input

Visit omega.com/omb-daq-2416

OMB-DAQ-USB-2416
Starts at
$1100

© Kutt Niinepuu / Dreamstime.com

Temperature and Humidity Virtual Chart Recorder

iTHX-W3 Series
Starts at
$295

Visit omega.com/ithx-w3

Wi-Fi Wireless Sensor System 802.11b/g Wireless Ethernet

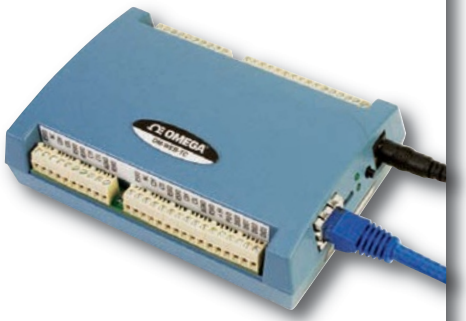
wSeries
Starts at
$195

wireless

Visit omega.com/wseries

8-Channel Web-Enabled Thermocouple Input Module

OM-WEB-TC
$599



MADE IN USA

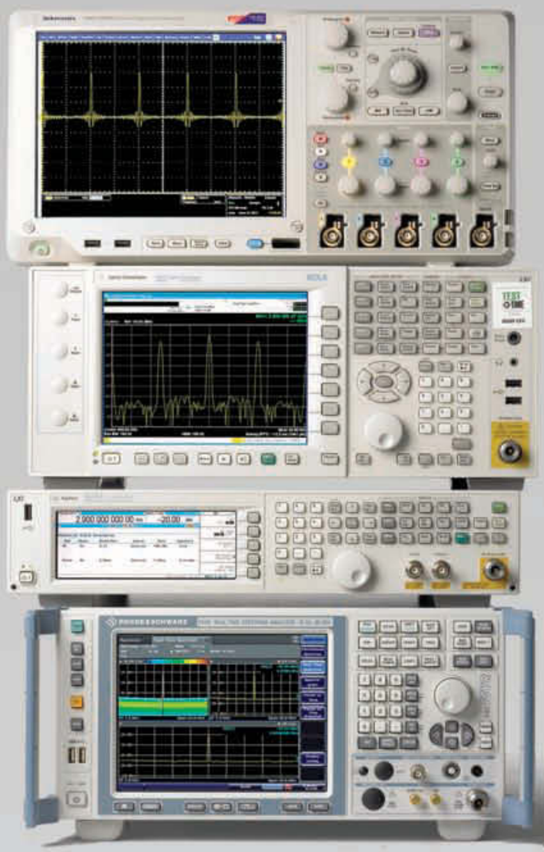
Visit omega.com/om-web-tc

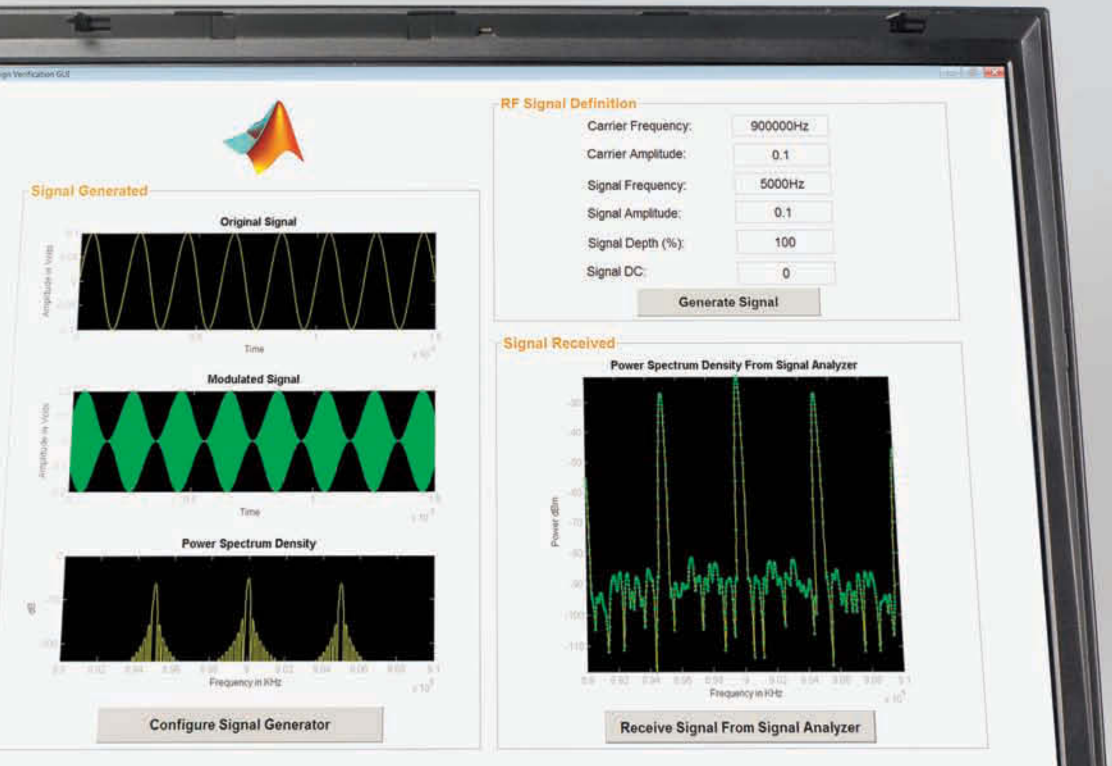
1-888-82-66342®
1-888-TC-OMEGA

Because of transmission frequency regulations, these wireless products may only be used in the United States and Canada (915 mHz models) or Europe (868 mHz models).

omega.com

OMEGA®





Generate Signal
Signal Generated
Original Signal
Amplitude in Volts
Time
Modulated Signal
Amplitude in Volts
Time
Power Spectrum Density
dB
Frequency in KHz
Configure Signal Generator
Signal Received
Power Spectrum Density From Signal Analyzer
Power dBm
Frequency in KHz
Receive Signal From Signal Analyzer

Cover story / Page 16

Test & MEASUREMENT WORLD®

MAY 2012
VOL. 32 NO. 4

CONTENTS

Product update / Page 38

FEATURES

SYSTEM INTEGRATION COVER STORY

16 **Integrating traditional and modular test instruments**

Numerous standards for instrument hardware and software must work together to form a complete automated test system.

By Larry Desjardin, Contributing Technical Editor

SIGNAL INTEGRITY

24 **Avoid a common S-parameter problem**

How you assign ports can greatly affect measurement interpretation.

By Eric Bogatin, Bogatin Enterprises, and Alan Blankman, LeCroy

RF PRODUCTION TEST

28 **Improve production test of high-speed RF components**

Using BER-SNR correlation, designers can test adjacent-channel rejection in VHF receiver ICs.

By Peter Sarson, austriamicrosystems

AVIONICS TEST

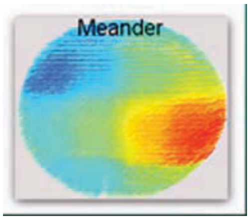
34 **Testing aircraft AFDX systems**

A new avionics communications network requires a test system that can monitor traffic and modify the data.

By William D. Wargo and Joachim Schuler, AIM

DEPARTMENTS

TEST DIGEST



VIEWPOINT

RENEW YOUR T&MW SUBSCRIPTION ONLINE: WWW.TMWORLD.COM/SUBSCRIBE

Online now at TMWorld.com

Check out these exclusive features on the *Test & Measurement World* Website:

Mods and rockers

"Mods" and "rockers" were two British youth subcultures in the 1960s whose interactions could turn violent. This epic rivalry is alive and well in test platform choices today. Why is there such polarization between supporters of modular and traditional instrumentation? Join the conversation! Post your opinion at:

bit.ly/HEHaGy

How long can you retrieve test data?

Many test instruments have long lives and require periodic calibration, and you must keep those records. If you use a paperless system for recording and storing test data, do you have systems in place that will work for the next 20 years? If you have test data stored on 5¼-in. floppy disks, do you have a machine that can read them?

bit.ly/IZ9rsK

Tips for testing processor cores

An IC integrator has many things to worry about, but testing the processor core should not be one of them. You can structure the test aspects of a core in a manner that makes them predictable. Ron Press of Mentor Graphics discusses a test strategy you can use:

bit.ly/HNhaJq

Go inside Fluke's electrical metrology lab

Fluke's Jeff Gust gave Martin Rowe of *T&MW* a first-hand look at the Fluke metrology lab.

bit.ly/Jo6FM7

Stay connected with *T&MW*

Join us for discussions about test topics:

LinkedIn: linkd.in/uRnG6r
Facebook: on.fb.me/vnV0ZB
Twitter: twitter.com/#!/TMW_Community

Test & MEASUREMENT WORLD

EDITORIAL STAFF

Director of Content: Patrick Mannion
patrick.mannion@ubm.com

Managing Editor: Deborah M. Sargent
deborah.sargent@ubm.com

Senior Technical Editor: Martin Rowe
martin.rowe@ubm.com

Senior Editor: Janine Sullivan Love
janine.love@ubm.com

Contributing Technical Editors:
Bradley J. Thompson, brad@tmworld.com
Shiv Balakrishnan, shivb1@gmail.com

Senior Art Director: Debee Rommel
Senior Production Editor: Laura Alvino

UBM EXECUTIVE OFFICERS

Chief Executive Officer, UBM Electronics, UBM Canon (Publishing), UBM Channel, and UBM Design Central: Paul Miller

Chief Executive Officer, UBM Electronics: Kathy Astromoff

Chief Information Officer: Brent Pearson

Chief Financial Officer, UBM Electronics & UBM Canon (Publishing): Jean-Marie Enjuto

Senior Vice President: David Blaza

Senior Vice President of Content: Karen Field

Vice President of Partner Services & Operations: Barbara Couchois

Vice President of Marketing: Felicia Hamerman

Director of Audience Engagement and Analytics: Amandeep Sandhu

HOW TO CONTACT T&MW

EDITORIAL:
33 Hayden Ave.
Lexington, MA 02421
Fax: 781-862-4853
E-mail: tmw@ubm.com
Web: www.tmworld.com

SUBSCRIPTIONS:
For address changes, cancellations, or questions about your subscription, please contact:

Customer Service
Test & Measurement World
P.O. Box 3609
Northbrook, IL 60065-3257
Phone: 847-559-7597
Fax: 847-564-9453
E-mail: tmw@omeda.com
Web: www.tmworld.com/subscribe

CIRCULATION:
Amandeep Sandhu
415-947-6301
amandeep.sandhu@ubm.com

LIST RENTAL:
Statlistics
203-778-8700

REPRINTS:
Wrights Media
877-652-5295
bkolb@wrightsmedia.com

Subscribe to T&MW online:
www.tmworld.com/subscribe

UBM Electronics
A UBM Electronics Publication

MARTIN ROWE
SENIOR TECHNICAL EDITOR
martin.rowe@ubm.com

20 years at *T&MW*

May 26 marks 20 years since I arrived at *Test & Measurement World.* Clearly, technology has changed over the last two decades. Most of the changes in test have come about because of changes in consumer electronics, namely computers and the Internet. Speeds of processors and signals have increased while time to market has decreased. Through it all, engineers are still faced with too little time and too few resources. Whether in good times or bad, there's always more work to do than people to do it.

When I started, engineers generally used DOS computers, although a few may have used Windows 3.1. Computer-based measurements meant using plug-in cards that ran on the ISA bus, but then the high-speed PCI bus soon replaced ISA.

Engineers who used to work entirely in the digital domain now have to learn how microwaves work.

Modular instruments consisted mainly of proprietary technologies. VXI looked like it would become the dominant backplane architecture and all automated test would adopt it. VXI, however, never became the replacement for GPIB that many marketers expected. Military and aerospace companies adopted VXI as a test platform, but few others did. PXI, which was introduced in 1997 and is morphing into PXI Express, has become the dominant open architecture for modular automated test systems.

Although modular instruments have grown as a platform for test, and other cabled buses such as USB, Ethernet, and Cabled PCI Express have been developed, GPIB is still holding on as a significant instrumentation bus. Why? It had a big head start, it's robust and reliable, and it has a huge installed base that will take many years to subside. GPIB, unlike consumer-electronic communications buses, is stable. It won't become obsolete, because newer versions probably won't come along to overshadow it. Sure, some new instruments come with USB and Ethernet ports only, but GPIB is still available as an option. Many new instruments, in fact, still have GPIB ports as a standard feature.

The Internet, and its demand for network bandwidth, keeps forcing serial-bus technology ever faster. It wasn't long ago (so it seems) that I was writing about testing optical data speeds at 622 Mbps. In less than 20 years, speeds like that are almost available to consumers. Today, 100-Gbps speeds are coming online with 400-Gbps speeds under discussion.

All those higher speeds mean ever-worsening signal-integrity problems. Engineers who used to work entirely in the digital domain now have to learn how microwaves work. You probably didn't think that would happen 20 years ago, did you?

Despite far better communications and the Internet, some things haven't changed. You probably still feel as though you don't have enough time, people, or equipment to do your job as well as you would like. In fact, you may feel more stressed because of acquisitions, layoffs, or budget cuts. That's certainly happened in the publishing business as well. Yet, despite being sold twice in 2010, we at *T&MW* are committed to bringing you the best technical content that we can. The delivery channels have changed and will continue to change, but quality content never goes out of style. T&MW

See the online version of this article to read more about the past 20 years of the test industry: www.tmworld.com/2012_05.

You work in all kinds of conditions, so should your spectrum analyzer.

Worst-case scenario: You've got minutes to troubleshoot RF interference that has shut down communications on the ground, at dusk, in the desert.

Best-case scenario: You've got the only spectrum analyzer with benchtop performance in a lightweight MIL-PRF 28800F Class 2 compliant handheld—with secure erase to keep classified data classified.

That's thinking ahead. That's Agilent.

Scan the QR code or visit http://goo.gl/Rfbde to see a HSA N9344C demo guide video

Handheld Spectrum Analyzers (HSA)

Key Specs	N9344C	N9343C	N9342C
Frequency	1 MHz– 20 GHz	1 MHz– 13.6 GHz	100 kHz– 7 GHz
DANL	-155 dBm/Hz	-155 dBm/Hz	-164 dBm/Hz
Sweep time	< 0.9 s	< 0.7 s	< 0.4 s
Weight with battery	3.6 kg (7.9 lbs)	3.6 kg (7.9 lbs)	3.6 kg (7.9 lbs)

Agilent and our Distributor Network
Right Instrument.
Right Expertise.
Delivered Right Now.

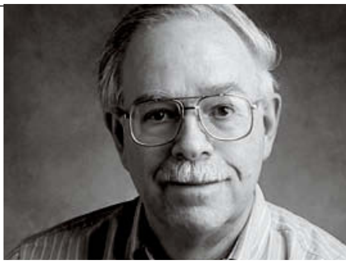
TESTEQUITY
800-732-3457
www.testequity.com/agilent

View online HSA video demos
Download demonstration guides
www.testequity.com/Agilent_HSA

Agilent Technologies

TESTVOICES

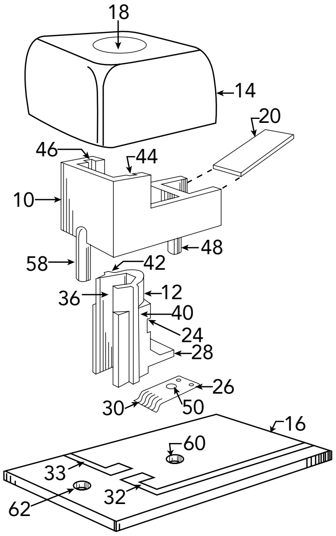
BRAD THOMPSON
CONTRIBUTING TECHNICAL EDITOR
brad@tmworld.com



5060-9436

That's the Hewlett-Packard part number for the front-panel push-button key switches used in the nonworking HP-8656B 0.1–990-MHz signal generator I recently added to my collection of obsolescent test equipment.

As received, all of the HP-8656's front-panel displays and indicator LEDs lit up like a Christmas tree. Replacing a missing low-voltage filter capacitor restored a normal display, but a subtler problem surfaced—one-third of the panel's 48 key switches wouldn't actuate or felt soft when pressed. An Internet search revealed the problem: The switches' return springs had collapsed.



The return spring is an elegantly simple steel leaf measuring 0.588 in. long by 0.140 in. wide by 0.002 in. thick. A slot in one end of the switch's red plastic body captivates one end of the spring. The spring's free end fits into a slot in the movable plunger. Pressing the plunger deforms the spring, providing an audible click and a restoration force when the plunger is released. The plunger's base forces a wiping contact across gold-plated printed-circuit board contact pads.

Reseating its spring repaired one switch, but examination revealed that springs in the remaining nonworking switches had either fractured or rusted through. Correspondents in Yahoo's HP-Agilent group offered a number of replacement suggestions, including trimming springs from stainless-steel shim stock, beryllium-copper EMI grounding fingers, and theft-prevention tags found in DVD packages. In some cases, dried lubricant residue within the switches also interfered with spring action. One group member generously sent me samples of his home-brewed replacement springs.

Hewlett-Packard used these key switches in other instruments, five of which in my collection amass an astounding total of 254 switches. Fortunately, none have yet collapsed.

I'm not complaining! This HP-8656B and other vintage instruments have long outlived their intended service lives and spare-parts inventories. Thanks to HP's enlightened policy of keeping service information available, plus a wealth of online support available from other users, I can coax a few more years of service out of what would otherwise be an unaffordable luxury for my workshop. T&MW

To read past Test Voices columns, go to www.tmworld.com/testvoices.

MORE SWITCH LORE

US patent 4,017,700 describes the leaf-spring key switch, known within HP as the "Bill West switch" after its inventor, and lists the spring as made from high-carbon steel (item 20 in Figure 6 at the following URL; see image at left):
www.google.com/patents/US4017700.pdf

NO MORE DINOSAURS

We'll eventually run out of older test instruments built with replaceable components and accompanied by service manuals and schematics, which manufacturers mostly no longer offer. Besides, after you locate a replacement for a 10-year-old custom-designed ASIC with hundreds of ball-grid-array connections, you're unlikely to replace it using a wood-burning pencil at the kitchen table.

Next-generation castoffs may include synthetic instruments. If we're fortunate, their building blocks will be interchangeable, and open-source control software will be available.

BUILD YOUR OWN!

Intrepid amateurs have successfully built versions of a DC-to-1-GHz spectrum analyzer design by Scotty Sprowls:
scottyspectrumanalyzer.com

Analog Devices' AD9850 DDS IC offers experimenters an inexpensive building block for RF signal generators:
www.qsl.net/pa3ckr/signalgenerator

As mentioned a few years ago by Martin Rowe, GPIB-Tcl offers an open-source alternative for controlling test instruments via the aging IEEE 488 bus (GPIB):
bit.ly/IO71sm

Download versions of GPIB-Tcl here:
gpib-tcl.sourceforge.net/GPIB-Tcl.html

Download the Tcl programming language and Tk GUI here:
www.tcl.tk

Researchers find semiconductor derivative of graphene

Researchers at the University of Wisconsin-Milwaukee have discovered a semiconductor that can be created from graphene. Graphene, crystalline carbon in the form of a single sheet of atoms, is expected to impact electronics because it offers higher electron mobility than materials used in silicon-based transistors. Until now, graphene and its derivatives have only existed as conductors and insulators.

The UWM researchers produced a derivative with oxygen atoms included within the hexagonal carbon-ring structure that characterizes graphene; they call their discovery GMO (graphene monoxide). The existence of the semiconducting derivative could help advance carbon-based nanoscale electronics, the university said.

UWM physics professor Michael Weinert and engineering graduate student Haihui Pu display a model of the atomic structure of GMO.

Photo by Alan Magayne-Roshak; courtesy of UWM.

The team discovered GMO while they were researching the behavior of a hybrid nanomaterial comprising carbon nanotubes with attached tin-oxide nanoparticles that was being investigated for use as a sensor. Professors Junhong Chen, Marija Gajdardziska, and Carol Hirschmugl collaborated on microscopy techniques to investigate carbon surfaces and to try to synthesize graphene from GO (graphene oxide), a multilayer insulator.

When heating GO in a vacuum to drive off the oxygen, the team found that layers of GO became aligned and formed GMO. The proportion of oxygen included can be varied, and at different high temperatures, the team produced four materials that they collectively refer to as GMO. bit.ly/IT01cQ.

Group to study reduced twisted-pair GigE

The IEEE has formed an IEEE 802.3 study group to explore the viability of reducing the number of twisted-pair wires used in Gigabit Ethernet PHYs (physical interface transceivers). Automotive manufacturers deploy IEEE 802.3 PHYs for applications such as data services, infotainment, and vehicle-control systems. Achieving GigE networking speeds via 1000Base-T for those applications would require four pairs of wires; reducing the number of wire pairs would cut the size and weight of Ethernet wiring in a vehicle.

"Reducing the number of wire pairs required to achieve high bandwidth could introduce additional, untapped markets for IEEE 802.3-based Ethernet technology, such as industrial-control and avionics, and have far-reaching impact across varied industries," said David Law, chair of the IEEE 802.3 Ethernet working group, in a prepared statement.

The group is slated to hold its first meeting during the IEEE 802.3 Ethernet Interim Session, May 14–18, in Minneapolis, MN. standards.ieee.org.

Editors' CHOICE

Agilent oscilloscopes reach 63 GHz

Agilent Technologies' Infiniium 96204Q DSO (digital storage oscilloscope) takes 160 Gsamples/s on each active channel with 63-GHz bandwidth when running on two of its four channels. The rms jitter noise floor is 75 fs. When the scope is running on four channels, the bandwidth drops to 33 GHz, because the four-channel mode allows the fastest members of each family to acquire 80 Gsamples/s simultaneously on all channels. The high bandwidths let users capture serial digital signals and perform eye-diagram analysis on 28-Gbps, 32-Gbps, and 40-Gbps digital signals.

Agilent has also introduced nine other four-channel oscilloscopes in the 90000Q series. The 10 instruments operate at five different bandwidths. Each model is available as a DSO or as a DSA (digital signal analyzer). Three pairs of instruments have bandwidths from 20 GHz to 33 GHz on two or four channels. The two pairs of higher-bandwidth models top out at 50 GHz and 63 GHz on two channels and 33 GHz on four channels.

The DSO versions come with 20 Msamples of waveform data while the DSA models come with 50 Msamples of memory. All models are upgradeable to 2 Gsamples of acquisition memory.

Price ranges: from $191,000 for the 20-GHz oscilloscope to $436,000 for a 63-GHz DSA. *Agilent Technologies, www.agilent.com.*

Read Dan Strassberg's full analysis of the 96204Q: bit.ly/HXbBEP.

CALENDAR

International Microwave Symposium, June 17–22, Montreal, QC. *IEEE, www.ims2012.mtt.org.*

SEMICON West, July 10–12, San Francisco, CA. *SEMI, www.semiconwest.org.*

EMC Symposium, August 5–10, Pittsburgh, PA. *IEEE Electromagnetic Compatibility Society, www.2012emc.org.*

Autotestcon, September 10–13, Anaheim, CA. *IEEE, www.autotestcon.com.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Editors' CHOICE

NI releases apps for LabView

National Instruments has released several mobile apps for iPhone, iPad, and Android devices that help engineers access data from data-acquisition and embedded-monitoring systems.

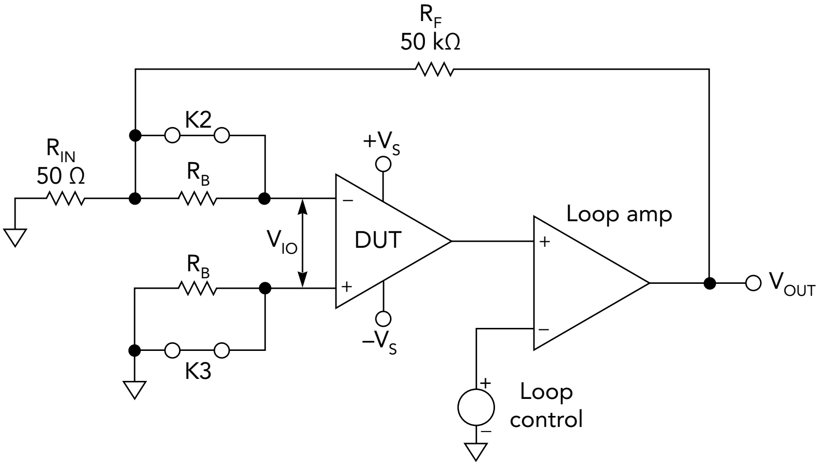
The Data Dashboard and the Data Dashboard Mobile apps for LabView enable users to view PC or embedded measurements from LabView using charts, text indicators, and LEDs. Users can also see distributed measurements from LabView-programmable devices, such as the NI CompactRIO system.

The NI cDAQ-9191 Data Display app offers connectivity to wireless NI CompactDAQ hardware for portable measurements. Users can configure and save measurements with a handheld device and can also program custom apps that connect to wireless NI CompactDAQ devices with the cDAQ-9191 Web API. NI has also released several other apps that display data-acquisition device pinouts and help users learn basic LabView concepts and common electric circuits.

National Instruments, www.ni.com/mobile.

OP-AMP TEST

Article series explains op-amp measurements



This circuit can measure bias current in either the inverting or noninverting input of an op amp.

Operational amplifiers require numerous measurements, both by their manufacturers and by the engineers who are designing them into circuits and systems. In a series of articles on www.tmworld.com, David R. Baum and Daryl Hiser of Texas Instruments explain which measurements are most important and how to make them.

In "The basics of testing op amps, part 1: Circuits test key op-amp parameters," Baum and Hiser cover measurements such as open-loop gain, offset voltage, common-mode rejection ratio, and power-supply rejection ratio. (Part 1 first appeared in the December 2011/January 2012 issue of *T&MW*.)

Part 2, "Test op amps for input bias current," explains that input bias currents produce errors in op amps. Data sheets often provide a table of bias currents for an op amp's noninverting (I_{B+}) and inverting ($I_{B–}$) inputs. The difference between these two inputs is the input offset current, I_{OS}.

You can use one of two circuits to measure bias current; the choice depends on the magnitude of the current. The circuit in the **figure** uses relays to configure the circuit for measuring I_{B+} and $I_{B–}$. To measure $I_{B–}$, close relay K3 and open K2. To measure I_{B+}, close K2 and open K3. The resistors labeled R_B can be replaced by capacitors for measuring low bias currents. Resistors work well for bias currents down to a few hundred picoamps. Below that, use capacitors.

In Part 3, "Configurable circuit tests op amps," Baum and Hiser use additional relays to form a reconfigurable circuit that can make all of the measurements described in part 1 and part 2. Part 3 opens with the complete circuit and then provides 12 different relay configurations with red traces that show the active circuit paths. Part 4, the final installment, will cover compensation issues that you must consider when using the test circuits.

You can link to the entire series at bit.ly/Hg63nW.

Martin Rowe, Senior Technical Editor

WAFER PROBING

High-temperature effects on wafer probing

Physical contact between the probes of a tester and the test pads of a device leaves marks on the pads (probe marks) that carry valuable information about the probing process, such as the accuracy of the probe placement on the pad. By analyzing these marks, manufacturers can discover the true performance of the prober, probe card, and setup under actual test conditions.

Manufacturers often use a time-consuming manual procedure to analyze probe marks, but new systems that perform automated probe-mark analysis can shorten the analysis time and deliver statistically valid quantitative data in an easy-to-interpret format. Automated analysis enables test engineers to rapidly assess the probing process, identify and analyze problems within the process, and define options for solving those problems.

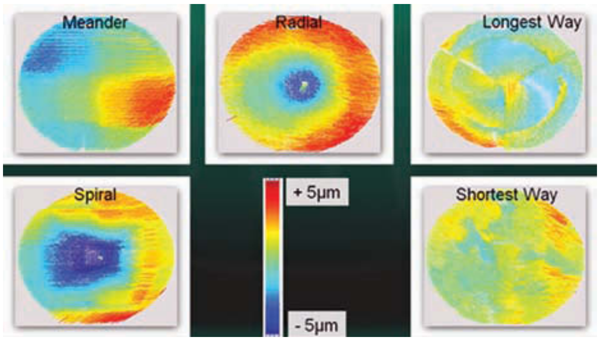
NXP Semiconductors manufactures high-performance mixed-signal and standard products used in various applications. Demand for testing at higher temperatures (200°C) on smaller pads prompted the company to perform a thorough evaluation of the probing process with three goals: review existing process settings for soak time and realignment to optimize probe-to-pad accuracy, evaluate external tools for probing-process analysis, and standardize probing-process analysis procedures within the company.

NXP evaluated a WaferWoRx (Rudolph Technologies) automated probe-mark-analysis system, comparing it to existing in-house techniques for analyzing the effects of soak time, stepping patterns, and prober realignments in a high-temperature production testing process. The company's engineers found that both the in-house method and the WaferWoRx system were capable of identifying testing-process errors, but the WaferWoRx system was also capable of collecting large amounts of data in a consistent way, and the data could be readily exported for additional analysis.

Using the system's automated capabilities and external analysis techniques, the engineers were able to select the stepping patterns and soak-time and realignment parameters that optimize probe-to-pad accuracy for test processes.

To read the full analysis of the system, see the online version of this article at www.tmworld.com/2012_05.

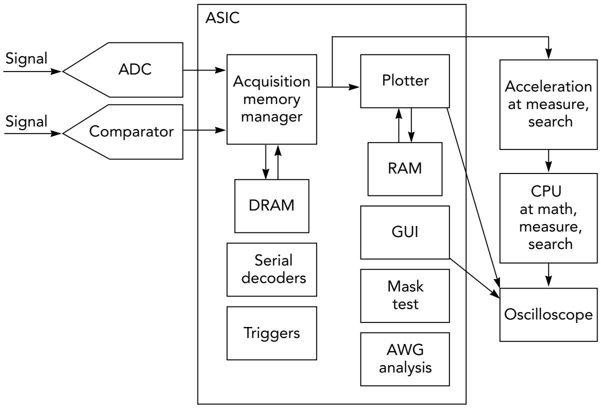
Darren James, Rudolph Technologies, and
Marcel Bleyl and Jan Martens, NXP Semiconductors



Probe-placement errors provide a means for estimating the relative goodness of a stepping pattern.

INSTRUMENTATION

Oscilloscope memory depth: when bigger is not always better



Unlike a CPU-based architecture, this architecture uses a custom ASIC to drive the plotting of waveforms from acquisition memory.

Oscilloscope memory depth is an often-misunderstood concept. In fact, many designers don't even know how much memory their scope has. When it comes to oscilloscope memory depth, bigger is always better, right? As with many things, the answer isn't as straightforward as it may seem.

The deeper the memory, the higher the sample rate will be as you move in to slower time/div settings. Maintaining high sample rate is important as it allows the scope to function at its maximum capabilities. Oscilloscopes that now offer 5-Gsamples/s sample rates also offer a wide range of memory depths, from 10,000 points (10 kpts) all the way up to 1 billion points (1 Gpts).

Deep memory is clearly beneficial when it comes to sample rate, but when would it not be advantageous? When it makes your oscilloscope so slow that it is no longer helpful in debugging a problem. Deep memory puts a larger strain on the system.

Some scopes are set up to handle that strain and will remain responsive with a fast update rate; others attempt to make memory depth a banner specification when it isn't really usable and slows the update rate by orders of magnitude.

The architecture of a sampling oscilloscope can impact the scope's performance. In some scopes, the CPU system is an integral block in the oscilloscope architecture ("CPU-based architecture") and is actually the gating item in how fast the scope can process the information and display it to the screen. If the CPU system isn't designed to handle deep-memory-acquisition records, it will need more time to process and display the data, therefore lowering the update rate of the scope (sometimes dramatically).

Scopes that are designed for deep memory, such as one that uses a custom ASIC that eliminates the need for the scope's CPU to be an integral part of the architecture, can provide faster update rates while maximizing memory and sample rate. You can link to my complete article on this topic from the online version of this article at www.tmworld.com/2012_05.

Richard Markley, Agilent Technologies

Integrating traditional and modular test instruments

Numerous standards for instrument hardware and software must work together to form a complete automated test system.

BY LARRY DESJARDIN, CONTRIBUTING TECHNICAL EDITOR

Test engineers have used open standard interfaces since 1975, when the IEEE approved IEEE 488, commonly known as GPIB. Since then, a spectrum of test-automation standards has appeared. These standards specify interface buses, modular formats, command languages, and software components. The breadth of choices makes the task of integrating instruments that use these different formats appear daunting. Fortunately, you can work through the challenges to develop automated test systems with improved throughput, measurement quality, and data analysis.

Hardware specifications include VXI, PXI, and AXIe modular formats. The LXI standard specifies an Ethernet communication standard widely adopted by traditional box instruments, and the IVI standards specify instrument software. (The **table** lists the full names of the communication standards used in this article.) In this article, I will explain how to use these standards to integrate modular and traditional instruments into a single test system, and I will focus on the controller interfaces and software required.

While this plethora of standards may seem to add complexity to a system, in some ways the standards are actually converging on two major interfaces: LAN and PCIe. Although GPIB is still widely used and will remain in use for some time, traditional "box" instruments have begun migrating to LAN, using the LXI protocols that transfer commands and data. Meanwhile, the three modular standards of VXI, PXI, and AXIe are converging on PCIe as the primary interface between the controller and the instrument: The VXIbus Consortium has recently adopted the VXI 4.0 specification that allows PCIe-based communication, PXI has been enhanced by PCIe for years, and AXIe uses PCIe as its principal interface. From a control and software point of view, communicating with any of these three modular instrument standards using PCIe is very similar and is nearly transparent to the system controller.

A third class of products—proprietary modular systems from a single vendor—doesn't conform to any of the three modular specifications. While modular in form, such systems typically behave more like traditional instruments that use LXI as an interface. For the purposes of this article, you can include them with the other traditional instruments.

Engineers must consider several factors when deciding whether to deploy traditional instrumentation, modular instrumentation, or a combination of the two. The key advantages of traditional instrumentation are the availability of nearly any type of product, the ease of use of the programming interface, and the ability to use the product as a manual bench instrument. Open modular systems typically offer smaller size, increased flexibility, and higher speed. The open-system aspect of the VXI, PXI, and AXIe standards lets you integrate products from different manufacturers within a single chassis.

For example, assume that a user has chosen to integrate two traditional LXI instruments with a PCIe-based modular chassis, either PXI or AXIe. **Figure 1** shows a simplified model of integrating traditional and modular instrumentation, using LAN and PCIe interfaces. It shows a controller with LAN interfaces for the traditional instruments, and a PCIe interface for the modular chassis. This is a logical model, not necessarily a physical model. With modular systems, the controller can be installed in the chassis. For the purpose of software integration, I'll consider the external interface model first and will return to the special case of the embedded controller later.

Review of the two interfaces

LXI is a set of protocols built on standard Ethernet. LXI instruments have a standard RJ-45 connector and offer 10-Mbps, 100-Mbps, and 1-Gbps Ethernet speeds. With 8 bits/byte, and some loss of bandwidth due to the Ethernet protocol, the equivalent speeds are approximately 1 Mbyte/s, 10 Mbytes/s, and 100 Mbytes/s, respectively. Though the interface on an instrument uses the same Ethernet specification as the LAN port on a computer, instruments are rarely connected directly to one another without an intervening router or switch.

PCIe is a computer expansion bus, largely designed for embedded computer peripherals and expansion slots inside a laptop or desktop computer or a rack-mounted controller. PCIe is essentially a high-speed serial replacement for the older PCI and PCI-X buses and uses shared address and data lines to all peripherals. A PCIe link can range from one to 32 lanes. Four-lane links are common in modular instrument systems, though some instrument slots may support more. A typical four-lane link offers 1-Gbyte/s transfer rates at Gen-1 (Generation 1) speeds, and twice that for Gen-2 speeds. To

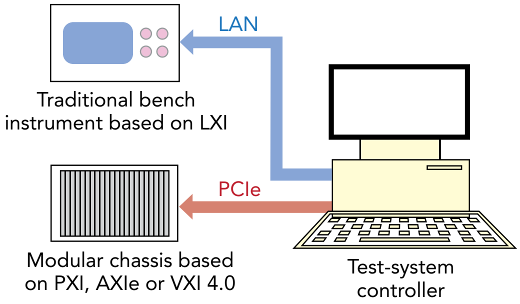


FIGURE 1. Two major industry standards now dominate instrument interfaces: LAN and PCIe. Traditional bench instruments, based on the LXI standard, are converging on LAN, while modular products are converging on PCIe.

connect externally, the PCIe must be buffered through a dedicated interface card.

Early PXI used the parallel PCI bus for data communication. With the advent of PCIe, the PXI standard was updated to take advantage of the higher speed and independent paths that PCIe offers. The PXI specification uses a clever architecture that lets the older PXI modules and the newer PXI Express modules (often denoted as PXIe) be integrated in a system. All AXIe systems offer PCIe as their data fabric. For the remainder of this article, I will refer to PXIe, AXIe, and VXI 4.0 products as PCIe-based products, since they are logically similar.

Message-based and register-based instruments

While PCIe delivers higher bandwidths than LXI, it is important to understand the true speed differences that result from the protocols commonly used with each interface. The differences between message-based instruments and register-based instruments create the fundamental tradeoffs between ease-of-use and speed.

Message-based instruments communicate through high-level, English-like commands sent by the controller to the instrument in a serial fashion. The most widely deployed command language is SCPI, which uses plain text for sending commands to instruments and for receiving responses. The IVI Foundation manages SCPI, which is designed so similar functions executed by different products and different vendors use the same command syntax.

Register-based instruments are completely different. The instrument is viewed as a set of registers in the controller's shared memory space. Reading from and writing to these memory addresses causes the instrument to execute the desired functions. These are often complex operations that are composed of many memory reads and writes and that often use bit-mapped registers and binary data. These complex operations are the equivalent of what occurs within a message-based instrument once it understands the SCPI command it has been asked to perform. Due to this complexity, register-based instruments typically are delivered with a software driver that executes the instrument function.

With few exceptions, LXI and GPIB instruments are message-based devices that use SCPI commands, and PXI and AXIe instruments are register-based devices that require software drivers. VXI instruments may be message-based or register-based. Indeed, the definition of message-based and register-based instruments first appeared in the VXI specification. For the purposes of this article, you should assume that all PCIe instruments are register based.

This difference between message-based and register-based devices is what creates the speed advantage in modular instruments. In a traditional message-based instrument, the SCPI command is sent as a set of ASCII characters, such as:

MEASure:VOLTage:DC? 10.0,0.001

This command requests that a DC voltage measurement be made with a maximum range of 10 V with 1 mV of resolution. The instrument, however, won't understand this English-like command. The instrument's internal processor must parse (interpret) a command to understand what is being requested. SCPI parsing typically requires milliseconds to execute.

The measurement is then executed by an internal register that accesses the instrument's hardware. Depending on the measurement, this may only require microseconds. The voltage measurement above can be performed in less than 100 µs, with the result in binary format. The instrument then builds the result as an ASCII number, and sends it to the controller. The controller converts the ASCII number back to binary to store or compare the result to limits. The entire process takes several milliseconds, even though the measurement only required microseconds.

For a register-based device, the process is completely different. A software driver is called that executes the register manipulations directly. The result is captured as binary data and directly used by the controller without conversion. Speed improvements of a factor of 50 have been demonstrated by using register-based instruments.

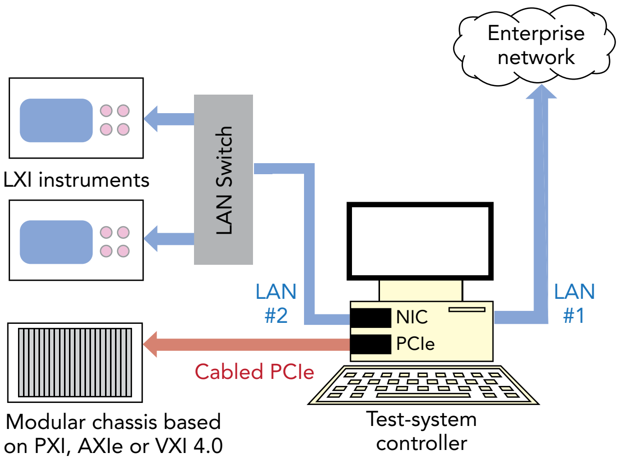


FIGURE 2. Two LAN connections are typically needed in a hybrid test system. One controls the test instruments, while another communicates with the enterprise network. Interface cards create a Cabled PCIe connection to the modular chassis.

sentinelEX

UNRIVALED PERFORMANCE
UNRIVALED SIMPLICITY

INTEGRATED DATA ACQUISITION SIGNAL CONDITIONING SYSTEMS

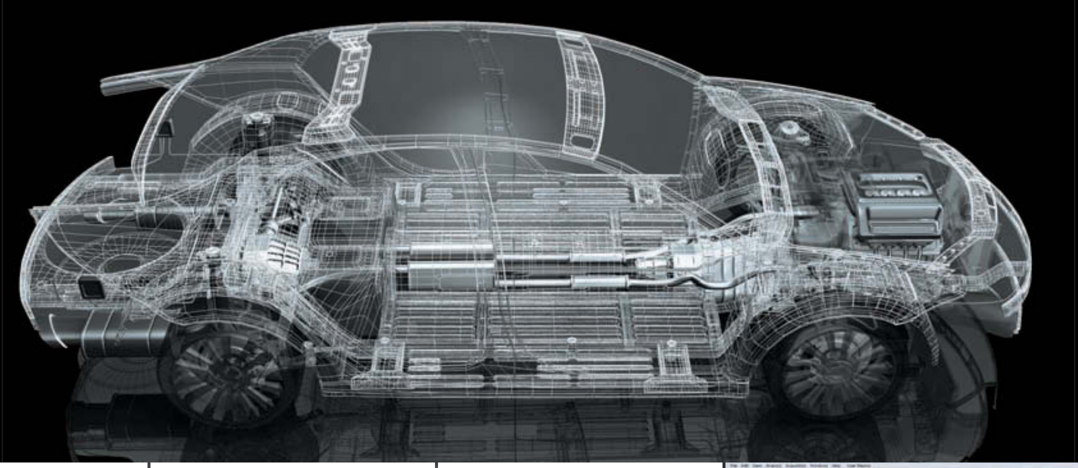
SentinelEX™, VTI Instruments' 4th generation of "Smart" dynamic and static data acquisition instrumentation, builds upon a proud legacy, established in the 1980's, by continuing to deliver trusted solutions to the marketplace.

Part of the largest worldwide install-base of precision data acquisition instrumentation, these innovative products are truly the gold standard for physical measurements, delivering unmatched confidence and performance.

- FPGA-based synthetic instrument customization
- Corporate wide "cloud" data management and access
- Flexible open architecture hardware and software designs
- Exceptional analog measurement and excitation performance
- Comprehensive health monitoring and run-time self-calibration
- Precision distributed measurement synchronization and control

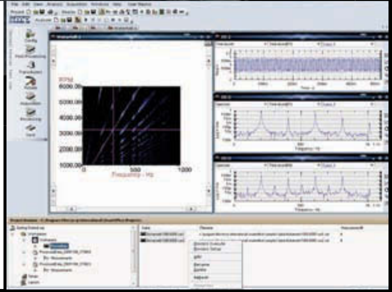
SentinelEX Series solutions are the perfect fit for a broad range of applications including noise, vibration and harshness (NVH), temperature, strain, voltage, parallel high-speed acquisition, and pyroshock.

DOWNLOAD COMPLETE SHORTFORM TODAY AT :
http://www.vtiinstruments.com/SentinelEX.aspx



VTI Instruments

High-Speed
Modal or GVT
Shock Testing
Vibration Testing
Order Analysis
Rotating Machinery
Acoustics
Temperature Monitoring
Structural and Fatigue



RELIABLE DATA FIRST TIME EVERY TIME

There is, however, an ease-of-use tradeoff. SCPI commands are easy to use and to read. They are also portable; they work in any operating system or automation environment. They avoid the need to deploy drivers, though drivers may be useful for other reasons. If measurement speed is not critical, or the measurement time is much longer than the command-interpretation latency, message-based instruments may be a good choice. For all of these reasons, many systems include a combination of traditional message-based instruments and high-speed modular instruments.

Integrating a hybrid system

The first part of integrating traditional and modular instruments in a hybrid system is the choice of interconnects and their configuration. LXI instruments will require the use of Ethernet. Note, however, that LAN networks are not all the same. It is rare to connect instruments directly onto an enterprise LAN. The data on an enterprise LAN would interfere with and slow down the real-time execution of the instrument control, while the instrument LAN would add significant traffic at the enterprise level. Typically, the LXI instruments will be placed on a completely different network than that used for the enterprise.

Thus, the controller will require two LAN interfaces—one connected to the enterprise LAN where the test plans and results are managed, and another dedicated to instrument control. An Ethernet switch is typically deployed from the controller to each instrument. This requires that a second NIC (network-interface card) be installed in the controller.

The situation is similar for PCIe-based modular systems. There is LAN communication from the controller to the enterprise, but the instrument communication occurs over PCIe. Most computers have PCIe internally. Unlike the LXI case, the instruments will be part of the same PCIe network and memory map as all the other computer peripherals, as this is where they get their speed.

The internal PCIe bus must, however, be buffered to avoid loading of these external instruments. Thus, you must install a PCIe interface card, which allows PCIe to be extended as a cable to a PXI, an AXIe, or a VXI 4.0 chassis. This electrically buffers the PCIe bus but keeps the same memory map. If a system uses multiple PCIe chassis, they will each require an additional interface card, or chassis extender. **Figure 2** shows a system configured with LAN and PCIe as the communication channels. The next step involves adding the required software.

Instrumentation software layers

Instruments, whether message-based or register-based, will require I/O commands. Even a simple SCPI-based instrument will need some way for the controller to send the command to the instrument. This is where VISA comes in. VISA is an industry-standard API (application-programming interface) for communicating with instruments from a PC. Versions of VISA are available from manufacturers of interface cards. VISA also allows communication to LXI instruments and PCIe memory-mapped instruments such as PXI, AXIe, and VXI 4.0.

Table. Instrument interface glossary

Acronym	Definition
AXIe	AdvancedTCA eXtensions for Instrumentation
GPIB	General Purpose Interface Bus, IEEE 488
IVI	Interchangeable Virtual Instruments
LAN	Local Area Network
LXI	LAN eXtensions for Instrumentation
PCI	Peripheral Component Interface
PCIe	PCI Express
PXI	PCI eXtensions for Instrumentation extension
SCPI	Standard Commands for Programmable Instruments
VISA	Virtual Instrument Software Architecture
VXI	VME eXtensions for Instrumentation

VISA, or an equivalent I/O library, is the minimum software needed to control message-based instruments. With VISA installed, you can program SCPI instruments using documented commands.

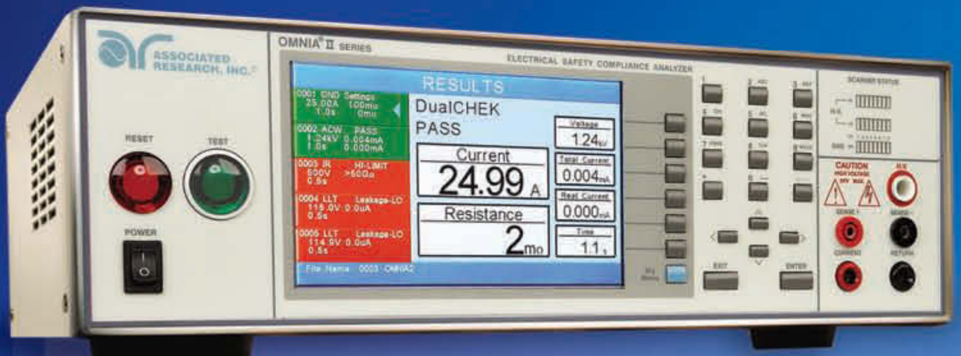
VISA by itself, however, is rarely enough to control PCIe instruments. You need the driver that creates the instrument functions. IVI drivers, based on standard APIs managed by the IVI Foundation, are designed to enable instrument control from PC environments.

The IVI drivers are designed to address two issues: They deliver the actual register operation that is the heart of the instrument function, and they ensure compatibility at the driver level between different types of instruments and between instruments from different manufacturers. Here, IVI leverages from SCPI by defining classes based on products types, which use APIs that look remarkably similar to SCPI commands. For instance, the equivalent IVI function call for a DMM (digital multimeter) may be:

```
dmm.DCVoltage.Measure (10.0, 0.001)
```

Because this call is done at compile time, little time is lost in the execution of the command. Command parsing isn't required at run time.

IVI drivers come in a number of variants, such as IVI-C and IVI-COM, optimized for different environments. PXI and AXIe products are nearly ubiquitously supported using IVI-C, which can be used in nearly any Microsoft automation environment, including the Microsoft Visual Studio environments, LabView, Matlab, and Agilent Vee. There are a number of shared components that must be installed at



ASSOCIATED RESEARCH, INC.
OMNIA® II SERIES
ELECTRICAL SAFETY COMPLIANCE ANALYZER
RESULTS
DualCHEK
PASS
Current
24.99 A
Resistance
2 mΩ
RESET
TEST
POWER

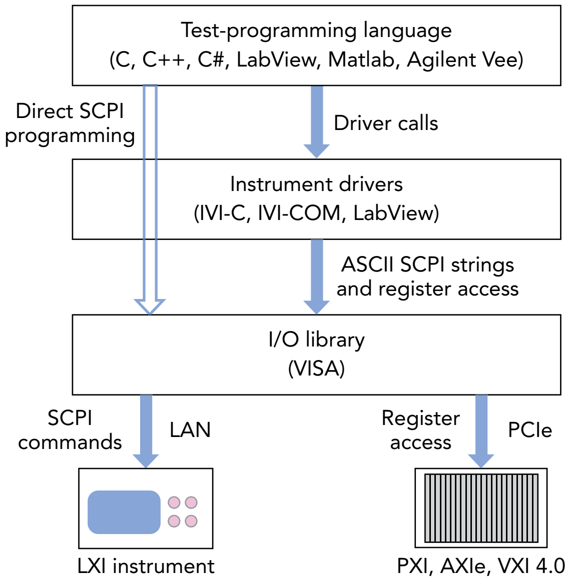


FIGURE 3. A test-programming language defines and sequences the tests, making high-level calls to the instrument driver. The instrument driver calls an I/O layer that sends the commands over a LAN or accesses the instrument registers over PCIe.

the same time to enable the IVI drivers. The IVI Foundation Website includes articles that provide details about the use of these drivers. Instrument makers can supply drivers more specifically tailored to work in the different operating environments. These may include LabView or Matlab drivers.

With the proper software drivers installed, the instruments can be programmed from the automation environment. The modular instruments are programmed using the chosen drivers. Though message-based instruments can be programmed directly in SCPI, many are controlled by the same IVI driver type that the modular instrument uses, such as IVI-C or LabView. This enables an additional level of consistency and allows for instrument substitution between traditional and modular form factors. **Figure 3** shows the software layers deployed in a hybrid system.

Embedded controllers

Up to this point, I have described the use of an external controller interfacing with LXI instruments and a PCIe-based modular chassis. But what if the controller is embedded in the modular system? What are the advantages and disadvantages of this approach?

The major change is that the PCIe interface that was needed to communicate to the modular chassis is essentially embedded in the modular controller. Other than that, the system architecture is the same. If the controller will control LXI instruments, there will need to be two LAN ports, one for the LXI control and one for the enterprise LAN, just as in the external controller case. Embedded controllers often have a spare expansion port that can accept a NIC or Cabled PCIe card.

One advantage to the embedded controller approach is that the system can be integrated into a mechanically smaller, lighter, and more transportable system. Another advantage is that the embedded controller will have been validated to work well as an instrument controller with robust PCIe enumeration.

Enumeration is the process by which a computer locates and identifies all PCIe devices. Many computers have not been validated for enumerating the deep PCIe tree structures that often are created with modular instruments. So, some instruments, though installed in the chassis, are not identified and cannot be controlled. This situation often needs to be resolved by the computer manufacturer with a BIOS update. Embedded controllers, through their design and extensive testing, are essentially guaranteed to perform the enumeration correctly.

A third advantage is enterprise governance. Even though a distinction between form factors does not seem valid to many engineers, embedded controllers are often accepted by an enterprise's IT department as deployable assets in instrument systems, while external computers fall under the regulatory auspices of the IT department. To prevent approval delays for purchasing external controllers, some engineers simply purchase embedded controllers.

At one time, there was a speed advantage with embedded controllers because their shorter bus lengths allow faster communication to the backplane. High-speed serial standards have all but removed this advantage, as Cabled PCIe to an external controller can deliver the same total bandwidth.

Embedded controllers do have some disadvantages. The first is cost. Instrumentation control remains a niche market compared to the consumer or industrial automation marketplace. Because of this, embedded controllers cost significantly more than their more common commercial counterparts.

The second disadvantage is performance. External commercial PCs often have the highest-performing processors and architectures, rapidly obsoleting their predecessors every few months. The embedded instrument controller market does not justify that level of investment, has fewer design cycles, and typically lags commercial PCs. Because of this, the highest-performance controllers will exist as stand-alone units and offer considerable cost savings. One common compromise is to deploy an industrial rack-mounted controller, which can have very high performance at competitive prices while requiring only 1U of rack space.

Another advantage of external controllers is expandability. External controllers offer any number of expansion slots, which can be used to control other peripherals or additional LAN or PCIe interfaces.

In summary, good instrument system design can allow a user to deploy the combination of traditional and modular instruments that best suits an application. In this article, I have focused on the computer system and software challenges and have presented options for creating a hybrid system. In a future article, I will explore the challenges and options in the electrical and mechanical aspects of integrating hybrid systems. T&MW


TS-900
Geotest
USB
USB

Avoid a common S-parameter problem

How you assign ports can greatly affect measurement interpretation.

BY ERIC BOGATIN, BOGATIN ENTERPRISES, AND ALAN BLANKMAN, LECROY

S-parameters, or scattering parameters, have become the de facto standard for describing the electrical properties of interconnects. They are one of the few concepts that bridge the worlds of the microwave designer, who typically lives in the frequency domain, and the digital designer, who typically lives in the time domain.

Everything you ever wanted to know about the electrical properties of an interconnect—a connector, a scope probe, a circuit-board trace, a circuit-board via, or a cable—is contained in the interconnect's S-parameters. But you need to use a consistent method for assigning the port index labels to inputs and outputs or you risk obtaining misleading S-parameter values, which will lead to incorrect interpretations.

Regardless of whether S-parameters come from measurements, circuit simulations, or electromagnetic simulations, the same formalism applies and the S-parameters behave the same. S-parameters describe how sine waves interact with and "scatter" from an interconnect. Each interconnect has "ports," defined as the ends of the interconnect into which signals enter and from which they leave. Each port has connections to the signal conductor and its return path. Index numbers label the ports into which a signal enters and from which it scatters.

Consistency is paramount when you are labeling these ports. Software used to calculate S-parameters uses a defined scheme to assign port designations, and you need to be consistent with that scheme. If you create S-parameter data-files based on one port-labeling scheme and use a data file that assumes a different labeling, the interpretation of the S-parameters and the results obtained using them will be wrong. This very basic issue of port assignment causes the most common problem when using S-parameter models: incorrect interpretation of the data.

By following one simple guideline, you can eliminate this problem. You will also be able to look at an S-parameter model and immediately determine if it assumed the incorrect port assignment.

Return loss and insertion loss

Each S-parameter is the ratio of the wave coming out of a port to the wave going into a port (**Figure 1**). The formalism of S-parameters describes the combination of sine waves scattered from the ports of an interconnect. Every combination of this input-output port ratio makes up an S-parameter's matrix elements. Each matrix element is defined by the input port number (the

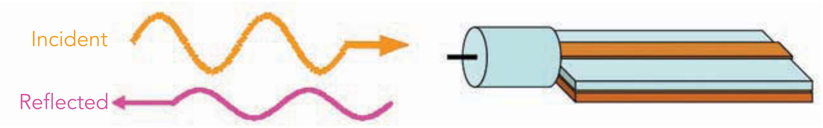


FIGURE 1. Each S-parameter is the ratio of a scattered sine wave from a port to an incident sine wave into a port.

stimulus) and the output port number (the response). This formalism applies regardless of whether the interconnect has just one port or 100 ports.

FIGURE 2. The return loss (red, S_{11}) and insertion loss (yellow, S_{21}) of a circuit board's transmission-line measurements show the characteristic behavior of return loss starting with a large, negative decibel value and an insertion loss starting with 0 dB at low frequency.

In a two-port interconnect such as a PCB (printed-circuit board) trace or a cable, there's only one way to assign the index port labels: port 1 on one side and port 2 on the other side. The S-parameter matrix element corresponding to a wave that goes into port 1 and reflects back out of port 1 is labeled as S_{11}. For historical reasons, S_{11} is also referred to as return loss. Because impedance changes along the interconnect cause reflected waves, return loss is very sensitive to the interconnect's impedance profile. The S-parameter corresponding to the wave going into port 1 and coming out port 2 is labeled S_{21} and is referred to, for historical reasons, as the insertion loss. It has information about reflections and is also sensitive to the losses in the interconnect.

One confusing aspect of S-parameters is the order of the index numbers used to label each S-parameter matrix element. If a signal were to go into port 1 and come out port 2, you might assume its label would be "S_{12}." The label would be easy to remember at a glance: The signal goes into port 1 and comes out port 2.

Unfortunately, as a consequence of the matrix math formalism, the labeling scheme follows the opposite structure. The S-parameter matrix element containing information about the wave going into port 1 and coming out port 2 is actually S_{21}.

At the lowest frequency, where the physical length of the interconnect is really short compared to ¼ of a wavelength, the reflection off the front of the interconnect and the reflection from the back end of the interconnect mostly cancel out one another, so the return loss, S_{11}, is nearly zero. In decibels (dB), the return loss for a through interconnect at low frequency is almost always a large negative decibel value.

The transmitted signal, described by S_{21}, is due to the initial transmitted signal, and a small contribution from the signal reflects off port 2 to port 1, then reflects back to port 2 and, finally, out port 2. At the lowest frequency, all of the signal gets through and comes out port 2. The insertion loss of a through-interconnect at low frequency will be close to 0 dB.

As frequency increases, the losses in all interconnects cause the insertion loss to fall, which means a larger and more negative insertion loss in decibels. An example of the measured return and insertion loss of a typical 50-Ω trace on a circuit board is shown in **Figure 2**.

This is an important observation: For virtually all interconnects, at the lowest frequency, you can expect the insertion loss to be nearly 0 dB. This is an easy and direct way to determine which matrix element is really the insertion loss, independent of the port labeling.

More than two-port S-parameters

Now comes the confusing part. If there are multiple interconnects, such as two adjacent transmission lines on a circuit board, there are two equivalent ways of labeling the port index numbers (**Figure 3**). In case 1, the opposite ends of one line are labeled port 1 and port 2, and the opposite ends of the other line are labeled port 3 and port 4. In this labeling scheme, the insertion loss of one line is still the S_{21} matrix element.

We recommend that you use the case 1 labeling scheme. It's consistent with the intuition we built up connecting insertion loss with the S_{21} matrix element, and it easily scales to more ports.

In case 2, port 1 and port 2 are the labels on the left side of the pair of lines and port 3 and port 4 are the labels on the right side of the pair. In this labeling scheme, the insertion loss of the first line is actually the S_{31} matrix element, and the near-end crosstalk is S_{21}.

Both labeling approaches are legal and used in the industry. Both ways are correct. The interpretation of the same-labeled S-parameter matrix element, however, is obviously different depending on which port assignment you use.

In the first port assignment, the insertion loss is S_{21} and you would expect it to be nearly 0 dB at low frequency. The S_{31} matrix element relates to the near-end crosstalk between the two lines and should always be very small, or a large negative decibel value at low frequency.

In the second port assignment, the insertion loss is the matrix element S_{31}. The matrix element S_{21} is the near-end crosstalk. These S-parameters are just as valid and just as well-defined as when labeled with the index port assignment of case 1. But if you use the S-parameter model created with one labeling scheme in an application that has a different labeling scheme, the result will be the same as if you had a bad model.

The way to tell which port assignment was used in an S-parameter file is to look at the S_{21} matrix element. If S_{21} looks like an insertion loss, starting out with a nearly 0 dB value at low fre-

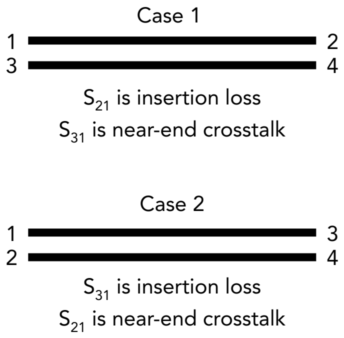


FIGURE 3. There are two approaches for assigning port labels to transmission lines. Case 1, the top approach, is the recommended approach. Case 2, although commonly used, is not recommended.

quency, then the port assignments were labeled as in case 1. If S_{31} looks like an insertion loss and has a nearly 0 dB value at low frequency, then the port assignments were labeled as in case 2.

As an example, **Figure 4** shows the measured S_{21} and S_{31} matrix elements from a pair of stripline traces. S_{31} looks like an insertion loss, starting out at low frequency with 0 dB. This S-parameter measurement used the second case as its port assignment. The S_{21} matrix element, looking like near-end crosstalk, is confirmation.

Knowing which port assignment was used is critical for two reasons. The end user of the model usually connects the S-parameter model into a circuit by connecting circuit nodes to ports. If the port assignments are not as expected, the circuit will still simulate and you will get a resulting waveform, but it will be a completely wrong result.

In addition, it is increasingly common for two single-ended transmission lines to be used as one differential pair. The differential insertion and return loss of the differential pair, designated by matrix elements SDD21 and SDD11, are created from linear combinations of the single-ended S-parameter matrix elements. If you assume the incorrect port assignments when calculating the differential S-parameters, the resulting differential S-parameters will be wrong.

To illustrate this problem, we measured the S-parameters from two stripline traces and stored them in a four-port S-parameter matrix using the case 1 port-labeling scheme. We then calculated the differential S-parameters in two ways: the first correctly assumed case 1 labeling; the second incorrectly assumed case 2 labeling. **Figure 5** shows the resulting differential insertion and return loss for each assumption.

FIGURE 4. The measured S_{21} and S_{31} matrix elements for two stripline traces show that the S_{31} element is clearly an insertion loss, confirming that the case 2 port-labeling scheme was used for this S-parameter matrix.

An insertion loss, whether single-ended or differential, will always start near 0 dB at low frequency. Clearly, the differential insertion loss assuming the wrong port assignment results in an insertion loss that is not consistent with our expectation, as it starts out with a large negative decibel value.

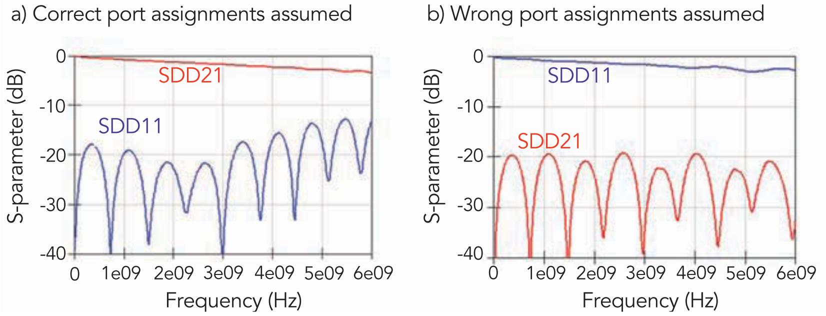
Recommendations for port assignments

Unfortunately, S-parameter files rarely note which labeling scheme was used to create the file, and you might forget to write down which scheme you used. If you deal with S-parameters from numerous sources, different files could have been created with different labeling schemes. This mix-up in the labeling scheme for the ports is the number-one source of confusion and the root cause of wrong results when using S-parameter models. (S-parameters are confusing enough without adding another opportunity for confusion.)

To avoid this common source of confusion, we strongly recommend you adopt the habit of labeling the port index numbers with odd port numbers on the left side and even port numbers on the right. This approach has two important advantages:

- It is consistent with the labeling of two-port interconnects. Insertion loss is still S_{21}.
- It is scalable, so for four ports, you just need to add the additional lines and continue with the labeling of 3 to 4, 5 to 6, 7 to 8, and so forth.

Regardless of which labeling approach you use, the first thing you should do when you get a new S-parameter data file is look at the S_{21} and S_{31} terms. If S_{21} looks like an insertion loss, you know the case 1 port-labeling scheme was used. If S_{31} looks like an insertion loss, you know the case 2 port assignment was used. If it is case 2, you can ask the engineer who created the S-parameter file to consider using a less-confusing port assignment in the future. T&MW


a) Correct port assignments assumed

b) Wrong port assignments assumed

FIGURE 5. When differential insertion loss and return loss are calculated from the same S-parameter file with two different port-labeling approaches, the results will differ. a) When the correct port assignments are assumed for the calculations, the insertion and return loss are consistent with expectations. b) When the incorrect port assignments are assumed, the insertion and return loss are clearly not correct.

Eric Bogatin *is a signal-integrity evangelist at Bogatin Enterprises, a LeCroy company. He holds an SB degree in physics from MIT and a PhD in physics from the University of Arizona in Tucson. He has been active in the signal-integrity industry for more than 30 years, writing articles and books and teaching classes. eric@bethesignal.com.*

Alan Blankman *is the technical product marketing manager for signal integrity at LeCroy. He holds a PhD in physics from the University of Pennsylvania and an MBA from the New York University Stern School of Business. He has more than 20 years of experience developing instrumentation and software for high-energy physicists and electrical engineers. alan.blankman@lecroy.com.*

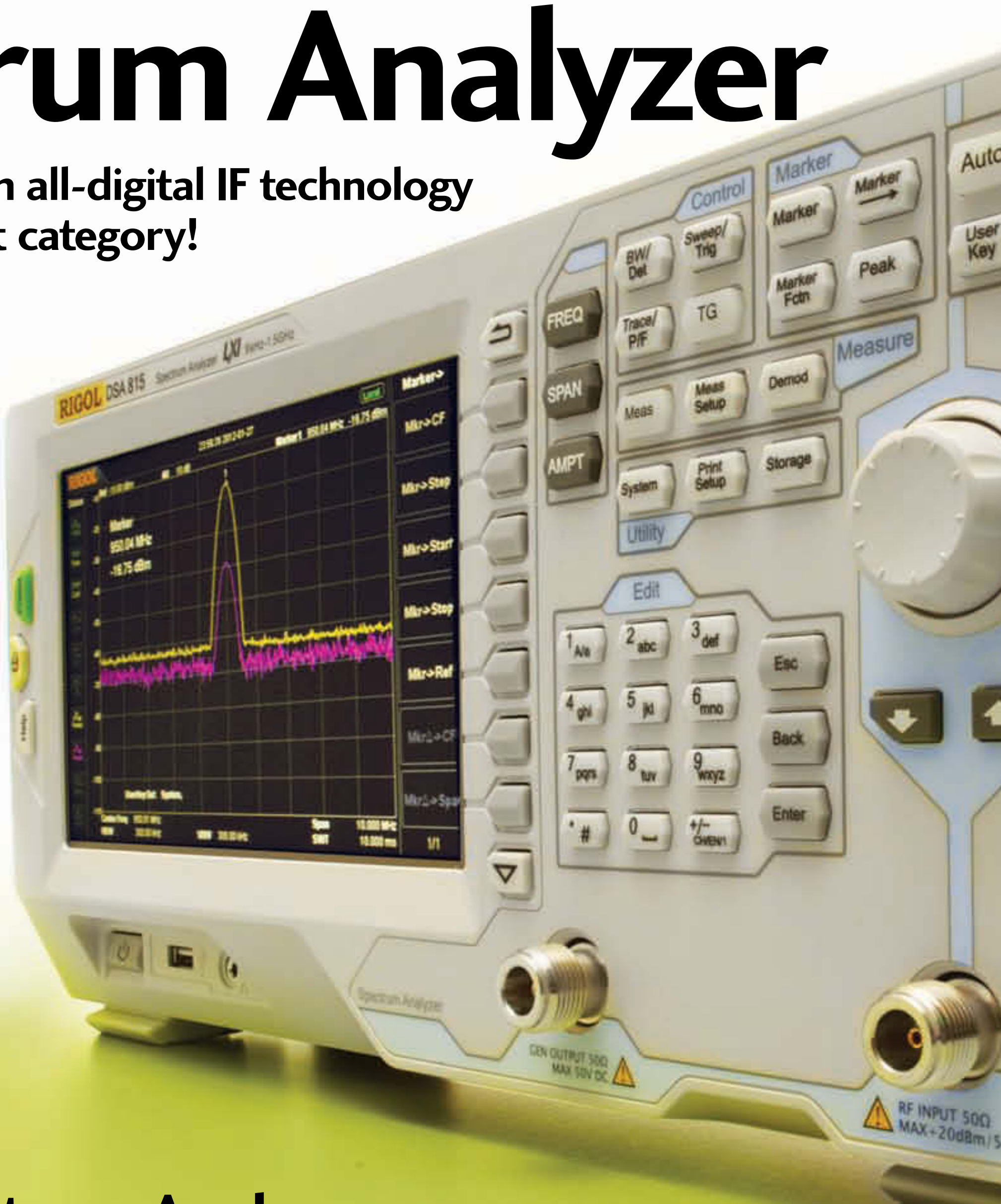
NEW! DSA815

Spectrum Analyzer

Our new analyzer with all-digital IF technology redefines the product category!

It's time to rethink your lab setup - because until now there's never been a spectrum analyzer that offered so much performance at a price you'd normally think of for an oscilloscope! The DSA815 Spectrum Analyzer covers a frequency range of 9kHz to 1.5 GHz and features a compact design and easy-to-use interface, making it ideal for benchtop or field apps in RF and wireless testing and production. Measure smaller signals with our digital IF filter that allows for smaller bandwidth settings and reduces displayed noise levels... and you can distinguish between signals with a frequency difference as little as 100 Hz. We include a wide range of standard functions including AM/FM demodulation and a preamplifier. And we offer some great options including an EMI filter and quasi-peak detector kit and a 1.5 GHz tracking generator.

Before your next compliance test, check out the DSA815... save one trip to the compliance lab and it pays for itself!



Now get a Spectrum Analyzer at oscilloscope prices

- 9 kHz to 1.5 GHz Frequency Range
- Typical -135 dBm Displayed Average Noise Level (DANL)
- -80 dBc/Hz @10 kHz offset Phase Noise
- Total Amplitude Uncertainty <1.5 dB
- 100 Hz Minimum Resolution Bandwidth (RBW)

Starting at

$1,295

Check out the Best Value in Analyzers, call 877-4-RIGOL-1 or visit RIGOLNA.com/DSA8

RIGOL
Beyond Measure

Improve production test of high-speed RF components

Using BER-SNR correlation, designers can test adjacent-channel rejection in VHF receiver ICs.

BY PETER SARSON, AUSTRIAMICROSYSTEMS

With BER-SNR (bit-error rate/signal-to-noise ratio) correlation, it is possible to test ACR (adjacent-channel rejection) in VHF receivers. Moving component testing for any device from the bench to production ATE (automatic test equipment) poses many challenges, but moving the testing of high-speed RF devices to a production setting can be downright daunting. To facilitate the testing of a VHF RF receiver in a production environment, you can employ a technique that correlates ACR in terms of BER to SNR. The technique, which was developed for ATE, greatly reduces test time and memory requirements while ensuring highly reliable test results.

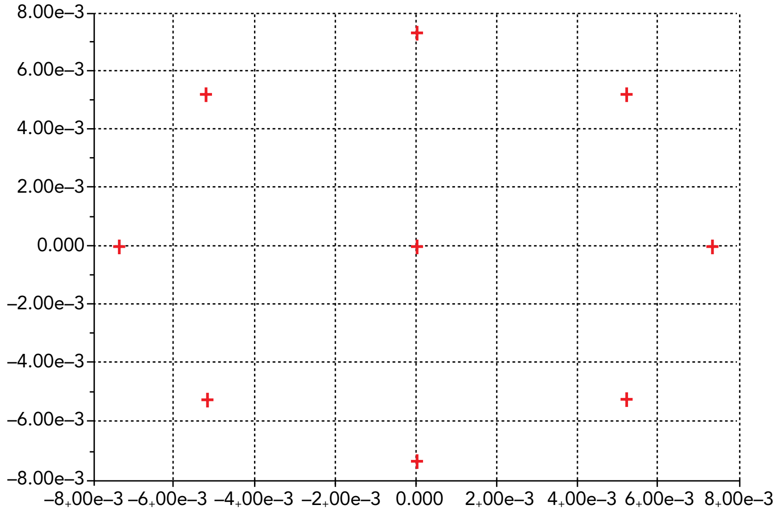


FIGURE 1. This DQPSK constellation diagram shows all of the constellation points that were extracted from the bench waveform.

During the development of an RF receiver (Rx), our team found that the performance was close to the limits of the customer's requirements. To make things more challenging, the performance demands on the receiver were continually increasing. We needed to accurately select devices close to the limits, or we would be rejecting otherwise good devices. This required an accurate and reliable test procedure that was also cost-effective for a production environment.

We undertook an exhaustive exercise to try to achieve good correlation from the test-bench setup to the intended ATE. The major problem was that we used a baseband device on the bench to downconvert the received digital RF signal, and a device was determined to be good or bad based on a result of the BER. To compound this problem, the specification that was close to allowable tolerance was ACR, which required two RF generators for the test-bench setup. Due to this complicated test approach, we could not

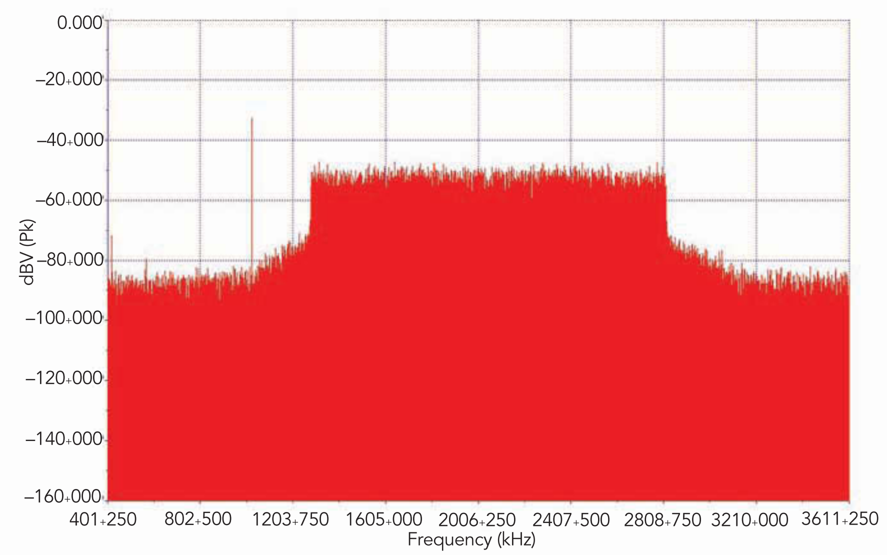


FIGURE 2. The OFDM receiver under test demonstrated typical in-band power levels for the wanted signal.

replicate the exact bench setup in our ATE environment, so we needed a new test technique for high-volume production testing.

Testing ACR

The ACR performance of a VHF receiver is based on a number of mechanisms, including image rejection, phase noise, and intermodulation distortion performance. All of these interact and cannot be treated separately.

The target application for this VHF receiver uses COFDM (coded orthogonal frequency domain multiplexing) signals that contain multiple carriers (many components at different frequencies), and they all interact. Unfortunately, it is not possible to accurately test the effect of the interaction of these subcarriers using single or dual tones. So, we developed a technique that uses representative signals in the unwanted adjacent channels and measures the noise generated in the wanted channel as a result.

We begin our ACR test by tuning the receiver to a low, wanted signal level and then having another signal present in the adjacent channel (upper or lower). The performance limit is reached when the power in the adjacent channel degrades the signal in the wanted channel by the amount that causes the BER specification to fail. Hence, the ACR is the difference between the wanted power and the adjacent power when the BER fails. By modulating one frequency generator on the ATE with the same modulation scheme used in the bench test setup, we were able to make a true comparison of the system performance.

Modulated waveform (COFDM)

Most bench setups use a modulation technique that resembles the real-world application, such as one containing several packets or frames of data. Due to test-time constraints and memory constraints of the hardware, sourcing and measuring this data at ATE rates is unrealistic. A full frame of data for this application would represent 96 ms of transmission time and require 12 Mbytes of memory.

Therefore, we decided to use two symbols of data for the modulating signal. That equates to approximately 320 kbytes of memory, which is still quite a large capture array for ATE. We selected two symbols with the greatest PAR (peak-to-average ratio) in order to detect the greatest effect on the device.

The RF generator needs to be adjusted based on the PAR of the signal in order to achieve the required output power. **Figure 1** shows the constellation of the two DQPSK (differential quadrature phase-shift keying) symbols that were extracted from the bench waveform.

Setting the generator to the same specified power level for the bench ACR test setup makes it possible to measure the power density in the specified bandwidth in terms of dBm/Hz at the center frequency of the DUT (device under test). The Rx design in this example demonstrated a power density of approximately −156 dBm/Hz in a 1.3-MHz bandwidth for a device with an ACR of 35 dB. **Figure 2** shows a typical OFDM (orthogonal frequency domain

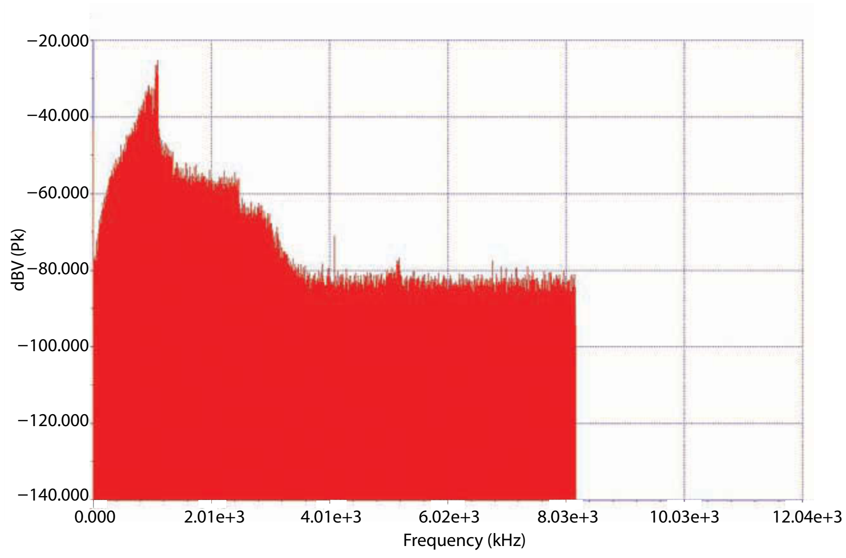


FIGURE 3. Unwanted signals from adjacent channels break into the desired band.

Solve Your Systems Needs

Fully Integrated Test Systems
Solutions For Any Application from DC to 50 GHz

Whether you choose one of our standard test systems – or have AR build a system to your specs – you'll be amazed at how easy, accurate, efficient, and affordable testing can be. Everything you need is right at your fingertips. It all works together perfectly, because everything has been carefully selected and assembled by AR engineers, using the most dependable and most innovative equipment on the market today.

Why An AR System Is The Smart Way To Test:

- No company has more experience and expertise in EMC test equipment than AR
- Reduced Test Time – get products to market faster
- Increased Accuracy
- Lower Risk
- Performance Guarantee – AR manufactures the majority of the system components allowing us to match and guarantee their performance
- Everything is fully tested before being shipped
- Single source for support & service
- More Compact & Portable – everything can be on one platform.

AR can deliver a solution that integrates all your testing needs: radiated immunity, conducted immunity, conducted emissions, radiated emissions, electrostatic discharge, lightning simulation … whatever you need.

We have the expertise and experience to supply turn-key and fully automated systems needed to test various standards including IEC 61000, MIL-STD 461 and 464, DO-160, wireless, automotive, HIRF and HERO.

To learn more, visit us at www.arworld.us or for technical support call 800-933-8181.

www.arworld.us/Systems

ISO 9001:2008
Certified

ar®

rf/microwave instrumentation

Other ar divisions: modular rf • receiver systems • ar europe

USA 215-723-8181. For an applications engineer, call 800-933-8181.
In Europe, call ar United Kingdom 441-908-282766 • ar France 33-1-47-91-75-30 • emv GmbH 89-614-1710 • ar Benelux 31-172-423-000

www.arworld.us

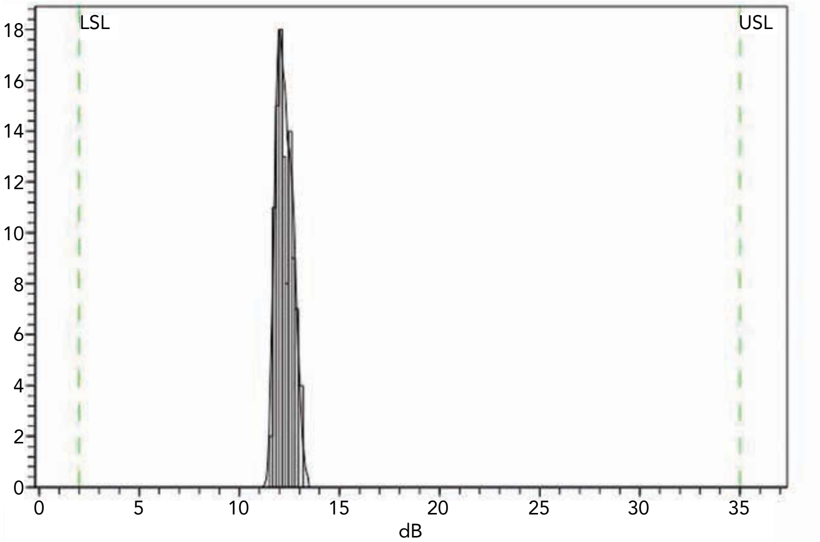


FIGURE 4. The ACR measurement is the difference between the wanted power and the adjacent break-through power

multiplexing) modulated spectrum from which the power was measured.

Keeping the device set to the same channel, the tester must shift the RF generator frequency to the adjacent-channel frequency and set the power to the expected ACR plus the original input power. The tester then needs to measure the power density again in the same specified bandwidth—that is, dBm/Hz at the center frequency of the device.

In this example, the tester measured a power density of approximately –169 dBm/Hz in a 1.3-MHz bandwidth for a device with ACR of 35 dB. **Figure 3** shows the power from the adjacent channel breaking into the "wanted" band. The ACR measurement is the difference between the wanted channel and the adjacent-channel measurements (**Figure 4**). Subtracting the two results reveals the SNR: –156 dBm/Hz – (–169 dBm/Hz) = 13 dBm/Hz.

After running the test 100 times, we calculated the standard deviation of this measurement and found it was 0.3 dB, which is extremely stable for a noise measurement. This low standard deviation was achieved by using the Unique Test Period averaging function of the LTX-Credence DIG-HSB digital-signal-processing instrument in the company's X-series testers.

A correlation graph that compares the actual measured difference between the in-band and out-of-band SNR shows that there is a good correlation to the ACR measured on the bench (**Figure 5**). This is due to accurately replicating the bench test setup, using the same excitation signal, and measuring the output in the same bandwidth that is being used in the application. This approach captured all of the influences, from phase noise to image rejection, that we saw on the bench. By using the same modulation technique and measuring the in-band power while the received signal is out-of-band, it is possible to achieve a good correlation to the bench test for ACR. T&MW

Peter Sarson *is the test development manager for austriamicrosystems' Full Service Foundry business unit. He received his BEng (Hons) from Sheffield University, UK, in 1998 and his chartered engineer status from the Institution of Engineering and Technology (formerly the Institution of Electrical Engineers) in 2003. He has worked in automated test engineering for 11 years.*

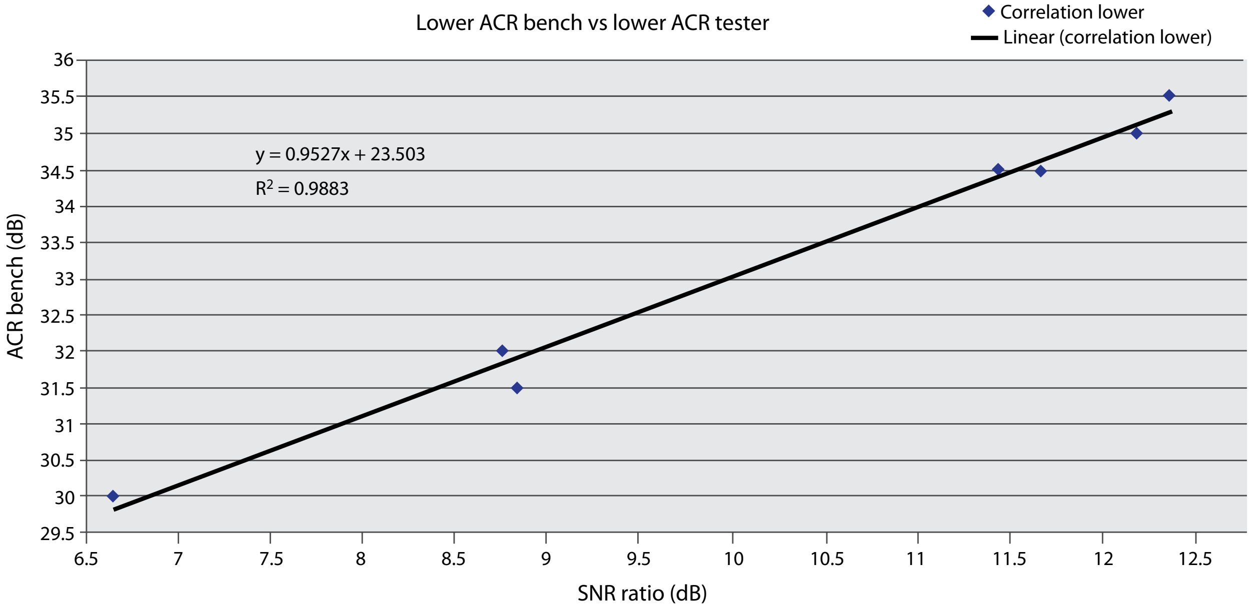


FIGURE 5. Correlation data compares the ACR measured on the bench to that measured on the ATE system.

Testing aircraft AFDX systems

BY WILLIAM D. WARGO AND JOACHIM SCHULER, AIM

A new avionics communications network requires a test system that can monitor traffic and modify the data.

Instruments in an aircraft typically communicate over an ARINC 429 data bus that uses simplex communication, supports data rates up to 100 kbps, and can transmit 23 bits of data with each message. If two instruments need to send data back and forth, then two ARINC 429 buses must be used. As a result, adding more devices that must communicate with each other quickly increases the number of necessary buses, and because of the low data-transfer rate, the amount of real-time data using this approach has to be kept to a minimum.

With the adoption of the AFDX (avionics full-duplex switched Ethernet) standard network, all devices can communicate on a single bus at much higher data rates (1000 times higher with the use of 100-Mbps Ethernet). This allows for much greater versatility and higher data throughput, so devices can communicate in real time. For the system designer, however, it introduces another set of challenges, since communications become time-division multiplexed and timing must be controlled.

The added complexity also creates a greater possibility for system-level problems, and the architecture of the bus, which includes multiple links and systems, makes it difficult to troubleshoot an issue. There is no simple method for monitoring all the data traffic, since multiple data paths are possible. This has led test companies to develop innovative tools for addressing AFDX test.

What is AFDX?

Using a special protocol to provide deterministic timing and redundancy management and to provide secure communications of data, AFDX is an avionics data network based on commercial 10/100-Mbps switched Ethernet. Its communication protocols were derived from commercial standards—IEEE 802.3 Ethernet MAC, IP (Internet Protocol), and UDP (User Datagram Protocol)—to achieve the required deterministic behavior for avionics applications.

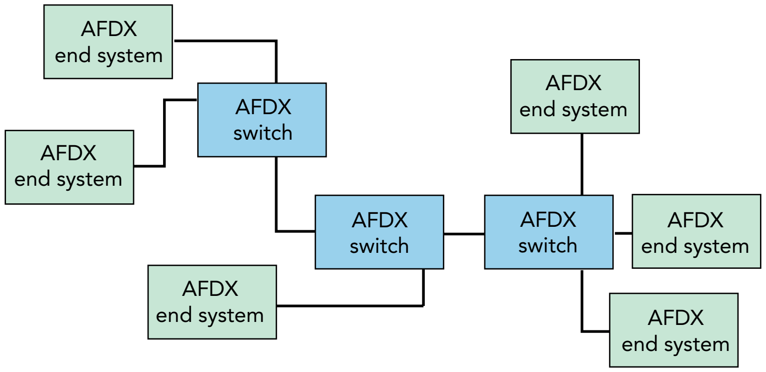


FIGURE 1. A typical AFDX system incorporates multiple switches and end systems.

AFDX is a registered trademark of Airbus, which has filed several patents around this technology. The technology has become accessible via the public ARINC 664 standard, which describes the core technology of AFDX. In particular, the end system and switch functionality is defined in ARINC 664 Part 7.

End systems, or LRUs (line-replaceable units), communicate based on VLs (virtual links) with traffic shaping through the use of BAGs (bandwidth allocation gaps), which are the minimum intervals between transmitted Ethernet frames on a VL. AFDX switches have functions for filtering and policing, switching (based on configuration tables), and end-system and network monitoring (**Figure 1**).

This new standard is already being deployed. The Airbus A380/A350/A400M, Boeing B787 Dreamliner, Comac ARJ21, and Sukhoi Superjet 100 all use AFDX data communications. In addition, AFDX and ARINC 664 Part 7 are being used as the backbone for all systems, including flight controls, cockpit avionics, air conditioning, power utilities, fuel systems, and landing gear. The first flight of the Airbus Industries A380 in April 2005 was a major milestone, because it was the first flight with AFDX on board that was based on the commercial 100-Mbps switched Ethernet with deterministic behavior.

Test systems for AFDX

The ideal test system for AFDX should be able to monitor all traffic, modify the data, and report results (**Figure 2**). A platform that combines a network "tap" (which can act in multiple modes), one or more dual-port simulation/analysis modules, and a set of software test tools running on a PC can perform all the necessary testing and troubleshooting. This

Measure Higher Bandwidth Signals.
All Software Compatible.

quickDAQ

DT9832

DT9836S

DT9862

Measuring high frequency component signals is straightforward using a USB data acquisition module with the appropriate Nyquist bandwidth. Each module has 16-bit resolution, 32 DIO, 2 C/Ts, and 3 Quad Decoders with simultaneous operation of all subsystems. quickDAQ application software allows data collection and analysis up to 10MHz and supports all modules.

Model	Analog Inputs	Analog Outputs	Throughput	Nyquist Bandwidth Max	±500V Isolation
DT9836S	6	0 or 2	800kHz/ch	400kHz/ch	✓
DT9832	4	0 or 2	1.25MHz/ch	625kHz/ch	✓
DT9832A	2	0 or 2	2.0MHz/ch	1.0MHz/ch	✓
DT9862	2	0 or 2	10.0MHz/ch	5.0MHz/ch	✓

800-525-8528
WWW.DATATRANSLATION.COM

DATA TRANSLATION®

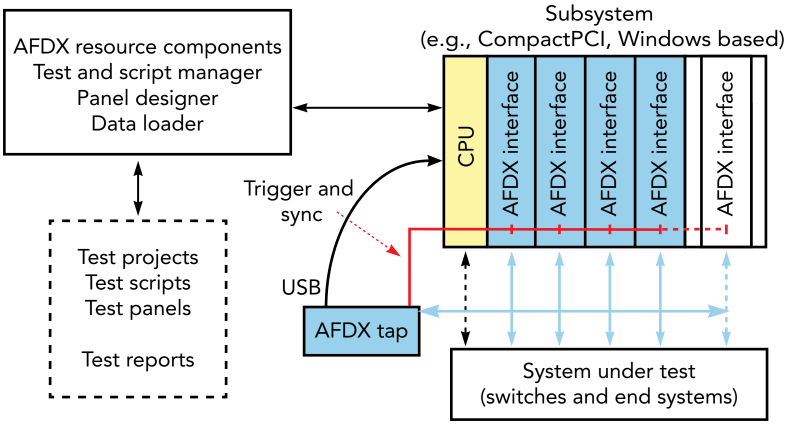


FIGURE 2. The ideal AFDX test system should be able to monitor all traffic, have the ability to modify the data, and be able to report results.

single configuration can monitor all traffic, modify and retransmit packets, change the destination of the packets, record data, convert the data into engineering units, and display the parameters.

Here are some valuable tools that an AFDX test system should include:

- **Tapping capability.** In-line monitoring of AFDX traffic can be useful when debugging networks. Compared to grabbing data from a monitoring port of an AFDX switch, in-line monitoring requires taps, which are ideally nonintrusive and can deliver time-stamped AFDX traffic representing the traffic as it appears on the line. Because AFDX defines redundancy by a duplication of the network connections ("red" and "blue" in Figure 2), in-line monitoring basically requires the monitoring of up to four Ethernet lines in total, two lines (Tx/Rx) per network connection. A tap such as the AIM fdXtap, for instance, can be used either to monitor one redundant AFDX network, up to two nonredundant independent AFDX networks, or even standard Ethernet networks.

The monitored lines need to be handled as four receive lines. Standard Ethernet test equipment offers taps but also often requires another four Ethernet ports to monitor the tapped traffic. With an AFDX-specific tap device, the four monitored Ethernet lines can be uplinked to a host via a USB 2.0 connection and integrated into the application software, where tapped data can be handled like traffic and received by an end-system simulation. Through synchronization, all generated (simulation interfaces) and capture traffic (by the tap) can be correlated.

- **Latency measurement.** When integrating complex AFDX and Ethernet networks with multiple switches, designers may become concerned about latencies. The capability of a network interface to transmit the time information, when the frame has been sent as part of the payload, allows a time-synchronized receiver to determine the latency through the network. Some AFDX and Ethernet tools offer such capability by default. For example, on the application and driver software level, frames can be configured accordingly on the transmitter side. All received frames are time tagged and the application software can decode them to deliver a measured latency time to the user.
- **Software.** Aircraft networks carry data that is used by end systems to perform time-sensitive critical tasks. Any error in communication or the interpretation of data can produce malfunctions of prime aircraft systems. As a result, it is as important to test end-system responses to both erroneous and valid data. It is not usually feasible to modify software in each of the various system components to introduce errors onto the bus. So, the best way to perform this testing is to have a "test" device in-line so that events on the bus can be modified at will to emulate error conditions.

One solution to this problem is AIM's REROS (re-routing software) functionality, which is executed on an AFDX interface board under control of an RTOS (real-time operating system). The functionality starts with a configurable re-routing of AFDX frames, based on VL numbers, to the network ports on the same interface board or to network ports of AFDX interface boards on the same backplane (PCI/CompactPCI). As a functional extension, the AFDX frames can be modified prior to retransmission in order to introduce physical errors or modify frame data (MAC addresses, IP header, UDP header, AFDX payload). Rerouting can happen as fast as possible or with a configurable delay, to compensate processing and transfer times when re-routing is done across several interface boards. The REROS functionality is typically supported and fully configurable using the corresponding application software

The transition from simple point-to-point systems to fully networked systems has provided a multitude of advantages to avionics systems designers. The added capability also has driven innovation in test techniques and tools. The first generation of AFDX systems saw the test methods develop concurrently with the systems to be deployed. Today, off-the-shelf hardware and software tools are available that can fully test and verify AFDX systems, and these tools can greatly increase efficiency in the development of new systems. T&MW

William D. Wargo, *president of AIM-USA, has been engaged in aerospace electronics for 30 years, working in engineering, business development, program management, and general management. Prior to joining AIM-USA, he held the position of VP of airborne telemetry for L-3 Communications, Telemetry-East Division. Wargo holds an MBA from LaSalle University and a BS in electronics engineering technology from Capitol College.*

Joachim Schuler *became the managing director of AIM GmbH in January 2010. He received his engineering and technical computer science degrees in 1991 and began his career in software development at Siemens Automation. After two years, Schuler joined AIM as a software development engineer. He became leader of the AIM software development team and served as technical leader and project manager for such projects as ARINC 664 end-system and switch-compliance test-system development and AFDX/ARINC 664 test-tools development.*

DEI SCIENTIFIC

IXYS SOLAR
Efficiency By The Sun

The accuracy you need at the touch of your finger™

How do you measure the power of GREEN™?

The PDG-3900

The SIV-3028

- 100MHz repetition rate
- 250pS delay adjustability
- Intuitive touch screen control
- GPIB, ethernet, RS-232 included
- Real time adjustability while enabled

- Automatically reads and calculates I_{sc}, V_{oc} and P_{mpp}
- Monitors and displays ambient light level in W/M^2
- Array, panel and individual cell measurements
- Compact and rugged for field use
- Touch screen operation

Call, E-mail or Visit
ixyscolorado.com
for information!
970.493.1901
sales@ixyscolorado.com

IXYS COLORADO

SPECIAL FOCUS: Production and Manufacturing Test

Keithley 2657A tests devices at 3 kV

Power semiconductors such as diodes, FETs, and IGBTs, particularly those made of SiC (silicon carbide) and GaN (gallium nitride), often need testing at high voltage both in the lab and in production. Keithley Instruments' 2657A high-voltage, high-power SMU (source-measure unit) can deliver up to 180 W of DC or pulsed power to a device under test. Its output can sink or source from ±3000 V at ±20 mA to ±1500 V at ±120 mA. That provides four-quadrant outputs.

Each 2657A has two pairs of ADCs (22 bit and 18 bit), one pair each for voltage and current measurements. The 22-bit integrating ADCs provide DC and low-frequency measurements while the 18-bit ADCs handle AC measurements with a sample rate of up to 1 Msample/s. The 22-bit ADC translates into a 6.5-digit multimeter that measures voltage, resistance, and current with a current resolution of 1 fA.

You can automate measurements using the 2657A's GPIB or Ethernet ports. Because it's LXI compliant, the 2657A has a built-in Web server so you can operate it remotely with a browser. For truly automated tests, you can use Keithley's TSP (test-script language) to run scripts in the instruments, calling them from a host computer. That computer can run an IVI-based driver or a LabView driver. You can also use Keithley's optional ACS Basic Edition software to characterize high-voltage or high-current devices.

When you need to test more than one device at a time, you can connect multiple 2657A's into a single system. Up to 32 instruments can be daisy-chained together through a pair of LAN ports on each instrument, with a host computer controlling the entire system connected either through LAN or GPIB.

Because the 2657A can produce up to 3000 V, it requires special safety precautions. To increase safety, Keithley offers the optional Model 8100 high-power device-test fixture. It contains double-redundant interlocks and grounding to ensure that the device under test can't float with respect to ground. That protects users against accidental overvoltage and overcurrent conditions.

Base price: $17,900; ACS Basic Edition software—$5000; 8100A test fixture—$6500. *Keithley Instruments, www.keithley.com.*

Multi-TAP JTAG controller fits Teradyne ICTs

Following the introduction of the USB-1149.1/CFM single-channel JTAG controller, Corelis has launched the QuadTAP/CFM, which integrates boundary-scan test capabilities into Teradyne in-circuit testers. Designed for the Teradyne TestStation and GR228X series of testers, the QuadTAP/CFM supports up to two TAPs with a single module and up to four TAPs using QuadTAP/CFM expander cards.

The single-slot custom functional module installs directly into one of the four slots on a Teradyne multifunction application board. According to Corelis, integration is simple and transparent. Once installed, the JTAG, GPIO, I2C, and SPI signals from the module are available directly to test fixtures and the tester backplane.

QuadTAP/CFM provides independently adjustable TAP interface voltages from 1.25 V to 3.3 V. It also offers a 100-MHz test clock rate for boundary-scan testing and is compatible with IEEE 1149.1 and IEEE 1149.6 digital networks. In-system programming of CPLDs and flash devices is accomplished through SPI and I2C interfaces.

Corelis, www.corelis.com.

USB module enables precise undersampling

Outfitted with two 16-bit simultaneous analog-input channels, the DT9862S USB data-acquisition module from Data Translation offers a bandwidth of 300 MHz and crystal-controlled sampling to allow low-jitter, precise undersampling. What's more, an external clock input enables you to lock the undersampling to a multiple of the signal under test.

In addition to the two single-ended analog inputs, the module provides two optional analog-output channels, 32 digital I/O lines, two counter/timers, and three quadrature decoders. You can achieve throughput rates of up to 10 MHz on one channel, 10-MHz burst sampling on two channels, or 5 MHz on two channels continuously. A ±500-V galvanic-isolation barrier prevents ground loops and maximizes analog signal integrity.

The DT9862S is available in a metal connection box with SMA connectors or as a board-level OEM device. A range of software options is offered at no additional charge, including drivers for Windows XP, Vista, and 7. DAQ Adaptor for Matlab and LV-Link for LabView are available for free downloading.

Base price: $3650. *Data Translation, www.datatranslation.com.*

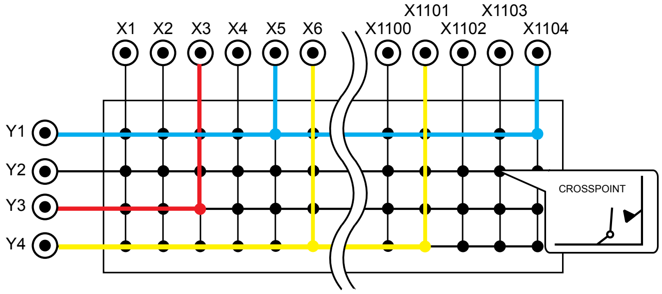
(continued)

PXI Matrix Switching

High Performance Scalable Matrix Solutions

BRIC™

Over 8 years experience and 100's of proven applications	✓
Highest Quality Reed Relays with ****SoftCenter*™ **Technology for maximum reliability	✓
Support for all major programming environments: all Windows versions, **LabView, SwitchExecutive	✓
Fault Insertion & ARINC 608A variants	✓
Highest PXI Switch density with up to 4416 crosspoints per module	✓



*SoftCenter is trademark of Pickering Electronics

**LabVIEW and SwitchExecutive are registered trademarks of National Instruments

Parameter	Pickering PXI BRIC	PXI Alternative
Integrated Analog Bus	Yes, Single or Dual Bus	Yes, Single Bus only
PXI Slots Occupied	2, 4, 8 Slots	4 Slot only
Choice of Relay Type to match your application	Yes, Reed Relay, Armature or Solid State. 1 or 2 Pole.	1 Pole Reed Relay only
Choice of Current Ratings	0.5A, 1A, 2A or 10A	0.25A or 1A only
Relay Self Test?	BIRST with milliOhm resolution and programmable resistance threshold	Pass/Fail
LXI Chassis Version	Yes	No, PXI only
Analog Bus Width	4, 8, 16, 32 pole	4, 8 pole
Warranty	2 Year	1 Year
Number of matrix module configurations	500+	< 20

Go to **www.pickeringtest.com/BRICadvantage/** and see all the choices available that can help make your next test system more flexible.

www.pickeringtest.com

Pickering Interfaces

Pickering Interfaces Inc., Grants Pass, OR. Tel: +1 541 471 0700
E-mail: ussales@pickeringtest.com
(East Coast Regional Office) Woburn, MA. Tel: +1 781 897 1710
Direct Sales Offices in USA, UK, Sweden, Germany, Czech Republic, France and China

pickering

Detailed Pricing & Technical Data On-Line

Multitest outfits pick-and-place handler for MEMS test

Multitest has expanded its MEMS portfolio to pick-and-place applications with the introduction of a test and calibration cart for the MT9510 series of pick-and-place handlers. MEMS solutions are available for strip test and singulated package test using the Multitest InStrip with the optional InCarrier, the MT93xx and MT9928 gravity test handlers, and now the MT9510XP (up to eight contact sites) and MT9510x16 (up to 16 contact sites) pick-and-place handlers.

Multitest, www.multitest.com/MT9510x16.

RF tester speeds testing of wireless products

RTX Technology has expanded its range of DECT/CAT-iq (cordless advanced technology) RF test platforms. The RTX2012 HS RF tester quickens testing of DECT/DECT 6.0/CAT-iq and Japan DECT systems. The RTX2012 HS, which can be used for a wide range of communication platforms, can operate as a stand-alone unit or as part of a testing system for production or certification.

The tester verifies the accuracy and stability of RF carriers and performs transmission-burst, bit-error-ratio, frame-error ratio, frequency-error, jitter, and packet-delay tests. The RF level output range is between –100 and –40 dBm; it can be adjusted on-the-fly for determining sensitivity of the device under test. The RTX2012 HS also supports audio loop-back by returning received audio signals to the device under test.

RTX Technology, www.rtx.dk.

Agilent releases test tool for Altair LTE chipset

Fully integrated and automated, Agilent's N7304A-2 application software and EXT wireless communications test set perform high-volume manufacturing test for equipment based on Altair Semiconductor's FourGee 3100/6200 TDD/FDD LTE chipset. The software can be used for RF calibration and verification of TDD/FDD LTE technologies for handsets, mobile devices, and customer-premises equipment. It also leverages the measurement science and sequence-analyzer techniques of Agilent X-series signal analyzers.

Agilent Technologies, www.agilent.com.

B&K Precision combines oscilloscope and AWG

B&K Precision's 2540B-GEN and 2542B-GEN combine a two-channel oscilloscope with an AWG (arbitrary waveform generator) in one unit. The 2542B-GEN is a 100-MHz oscilloscope with a function generator capable of producing 40-MHz sine waves, while the 2540B-GEN is a 60-MHz oscilloscope with a 20-MHz AWG. Both oscilloscopes sample at rates up to 1 Gsample/s on one channel or 500 Msamples/s on two channels. Standard memory depth is 16 ksamples for one channel and 8 ksamples/channel on two channels.

Both models have math functions such as add, subtract, multiply,

COMING TO A CITY NEAR YOU!

2012 X-fest

From April through September 2012, Avnet and Xilinx will co-host X-fest technical training events throughout Asia, Europe and North America.

X-fest's in-depth curriculum offers a full-day of practical, how-to training for FPGA, DSP & embedded systems designers. The fully-customizable training experience allows attendees to pick up to four courses from any of the three unique training tracks.

FPGA Fundamentals Track

The FPGA Fundamentals track focuses on common design issues facing both new and advanced FPGA designers.

Applications Track

The Applications track delves deeper into design methodologies and techniques required when designing with the Zynq™-7000 Extensible Processing Platform (EPP) and 7 series FPGAs.

Zynq-7000 EPP Track

The Zynq-7000 EPP track provides four courses dedicated to the ARM® dual core Cortex™-A9 MPCore™ based device.

Register for a FREE ALL ACCESS PASS

budurl.com/2012Xfest

PARTNER DEMONSTRATIONS AND EXHIBITS

Xilinx
Avnet
Analog Devices
Maxim
Micron
TE Connectivity
Texas Instruments
Cypress Semiconductor

Aldec
ARM®
MathWorks
Spansion
FCI
Samtec
PLDA
Ericsson

XILINX® 2012 X-fest AVNET®

Learn more at **budurl.com/2012Xfest**

DON'T MISS ANY X-FEST UPDATES. JOIN THE CONVERSATION TODAY!

@avnetxfest
facebook.com/xfest2012
Join the Avnet X-fest group!

divide, and FFT, letting you derive information not apparent from just a captured waveform. Other measurements include min, max, rise/fall time, average, rms, and overshoot. Cursors let you calculate differences in amplitude and time between two points.

The instruments have remote-control capability through their USB, LAN, and RS-232 ports. Using the LAN port, you can operate the instrument with a browser. All communication ports use the company's Comsoft software for remote operation. A front USB port lets you connect a flash drive for data storage. The rear panel also includes a pass/fail digital I/O port.

Prices: 2542B-GEN—$1395; 2540B-GEN—$1195. *B&K Precision, www.bkprecision.com.*

LeCroy rolls out WaveStation generator line

WaveStation two-channel function/arbitrary waveform generators from LeCroy offer bandwidths of 10 MHz, 25 MHz, and 50 MHz; a sampling rate of 125 Msamples/s; and 14-bit resolution. They also provide 16 kpoints of memory per channel and a 3.5-in. color display for previewing waveforms.

In addition to basic functions, such as sine, square, ramp, pulse, and noise, WaveStation generators have more than 40 built-in arbitrary waveforms. The large display lets you view waveform shape, along with various parameters, including frequency, amplitude, offset, and phase. The instruments also furnish AM, PM, FM, ASK, PSK, FSK, PWM, and other modulation schemes that can be controlled using the front panel. All necessary I/O connections for synchronizing the dual output are accessed on the rear panel. USB and IEEE 488 interfaces are standard.

The accompanying PC software simplifies waveform creation and editing. Waveforms can be created, shaped, and edited using mathematical operators or digital filters, or by placing individual sample points. The software also supplies a flexible waveform-drawing tool that allows you to create a free-form waveform sketch on the PC and output it from WaveStation.

Introductory prices: 10-MHz model—$990; 25-MHz model—$1950; 50-MHz model—$3450. *LeCroy, www.lecroy.com.*

Fluke thermal imagers find hot spots

Fluke's new line of thermal imagers, the Models Ti100, Ti110, and Ti125, let technicians find trouble before it occurs. Machines and electrical components may experience a rise in temperature before they fail, and infrared thermography can detect those temperature rises. The photo of a Ti100 shows three circuit breakers, one of which is hotter than the others (shown in red). Thus, it's dissipating excess energy and could potentially fail.

The three thermal-imager models vary in specifications, but all provide color images of temperature that's visible on the screen or can be downloaded to a computer through a USB link. The instruments can also store images on SD memory cards, capturing up to three digital photos per thermal image (Ti110 and Ti125 only), and you can annotate images for documentation. The general-purpose Ti100 and the

LXI
Agilent
EXG Vector Signal Generator
N5172B
9kHz-6GHz
EXG
FREQUENCY
6.000 000 000 00 GHz
AMPLITUDE
20.00 dBm
I/Q Routing & Optimization
I/Q Adjustments: Off
BB GEN
EXT IN
I/Q OUT
RF OUT
Optimized Path
I/Q Source (Internal)
I/Q Correction Optimized Path (RF Output)
I/Q Adjustments (Off)
I/Q Calibration
More 1 of 3

industrial-grade Ti110 cover a temperature range of –20°C to 250°C, while the industrial-grade Ti125 covers –20°C to 360°C. The models Ti110 and Ti125 also include a 2-Mpixel digital camera for documenting the thermal images.

When designing the imagers, Fluke focused on one-handed operation. Weighing 1.67 lb, the imagers are designed to balance in your hand and can be operated with or without gloves. You can also operate the imagers either horizontally or vertically for long periods. The imagers come with a 2-Gbyte SD memory card, an AC battery charger, a handle that you can attach to either side of the unit, a USB cable, and a carrying case. The Ti125 comes with a spare lithium-ion battery.

Prices: Ti100—$2495; Ti110—$4495; Ti125—$5495. *Fluke, www.fluke.com.*

Boundary-scan package integrates digital oscilloscope

XJTAG and Pico Technology have joined forces to produce XJTAG Expert, an integrated JTAG boundary-scan oscilloscope in a portable package that requires just two USB connections. The PC-based device employs a USB 2.0-to-JTAG adapter to provide a high-speed interface to the JTAG chain on a target circuit board while leveraging advanced digital features for debug, test, and repair. It also comes with a self-contained license so you can use XJTAG Expert on multiple PCs.

XJTAG Expert combines the functions of a digital oscilloscope, spectrum analyzer, waveform and function generator, and serial protocol analyzer. The 200-MHz oscilloscope provides two channels, a 128-Msample buffer memory, 8-bit resolution, and 500-Msamples/s real-time sampling. An ETS (equivalent time sampling) mode boosts the maximum effective sampling rate to 10 Gsamples/s to deliver a more detailed display of repetitive signals.

The spectrum analyzer allows signals up to 200 MHz to be viewed in the frequency domain, while the function generator produces signals such as sine, square, triangle, and DC level. A built-in AWG editor enables waveforms to be created or edited, imported from oscilloscope traces, or loaded from a spreadsheet. In addition, you can use XJTAG Expert to analyze CAN, I2C, SPI, RS-233, and UART protocols.

Along with test clock frequencies of up to 166 MHz, XJTAG Expert accommodates up to four TAP connections to the unit under test, as well as different cable and board configurations. Since the unit is USB-powered, it requires no external power supply. XJTAG Expert can also supply power to small target boards (3.3 V, <100 mA) to enable testing without a main source of power.

XJTAG, www.xjtag.com.

Anritsu introduces tri-wavelength OTDR modules

The µOTDR modules for Anritsu's Network Master MT9090A platform provide the tools needed for installing and maintaining optical networks, including PON-based FTTx networks with up to a 1×64 split. The MU909014C and MU909015C modules provide three wavelengths: 1310 nm and 1550 nm for installation and either 1625 nm or 1650 nm for maintenance.

Each of these modules combines an OTDR, power meter, light source, loss test set, PON power meter, and connector-inspection microscope in a pocket-sized package. The µOTDR modules offer a dynamic range of up to 38 dB to ensure accurate fiber evaluation of any network, including premise, access, metro, and core. The modules also feature up to 250,000 sampling points, a sampling resolution of 2 cm, and dead zones of less than 1 m. A customizable test sequence and full auto mode can be used to automate testing and guide novice users. The Network Master MT9090A mainframe is outfitted with a 4.3-in. TFT color LCD and dual USB ports for easy data transfer.

Anritsu, www.anritsu.com.

Test & MEASUREMENT WORLD

BUSINESS STAFF

Senior Vice President, UBM Electronics:
David Blaza, david.blaza@ubm.com

Vice President of Partner Services & Operations:
Barbara Couchois, barbara.couchois@ubm.com

Senior Director, Interactive Media:
Laura Lang-Dacus, laura.lang@ubm.com

Interactive Media Manager:
Stephaney McGinnis, stephaney.mcginnis@ubm.com

Vice President of Marketing:
Felicia Hamerman, felicia.hamerman@ubm.com

Marketing Project Manager:
Esther Aronov, esther.aronov@ubm.com

ADVERTISING SALES

Eastern and Central US; Canada:
James Leahey, 262-656-1064; james.leahey@ubm.com

CA, CO, TX, and Northwest US:
Donna Marlett, 310-445-4213; donna.marlett@ubm.com

Germany, Austria, Switzerland:
Adela Ploner, Schondorf am Ammersee, Germany.
+49-8192-933-78-22; adela@ploner.de

PRODUCTION STAFF

Senior Vice President, Strategic Development and Business Administration: Pat Nohilly

Senior Vice President of Manufacturing:
Marie Myers, marie.myers@ubm.com

Senior Distribution Director:
James Pizzo, james.pizzo@ubm.com

Production Director:
Donna Ambrosino, donna.ambrosino@ubm.com

Production Manager:
Robert Steigleider, robert.steigleider@ubm.com

VOL. 32, NO. 4

Subscription Policy: Test & Measurement World® (ISSN 0744-1657) is published monthly except January by UBM Electronics, 600 Community Dr., Manhasset, NY 11030-3825. Periodicals postage paid at Manhasset, NY, and additional mailing offices. SUBSCRIPTIONS: Free to qualified subscribers as defined on the subscription card. Rates for nonqualified subscriptions, including all issues: 1 yr. $150, 2 yrs. $250, 3 yrs. $300. Except for special issues where price changes are indicated, single copies are available for $10 (US orders) and $15 (foreign orders). Buyer's Guide issue is available for $35 (US orders) and $40 (foreign orders). For telephone inquiries regarding subscriptions, call 847-559-7597. E-mail: tmw@omeda.com. CHANGE OF ADDRESS: Notices should be sent promptly to P.O. Box 47461, Plymouth, MN 55447. Please provide old mailing labels as well as new address. Allow two months for change. NOTICE: Every precaution is taken to ensure accuracy of content; however, the publishers cannot accept responsibility for the correctness of the information supplied or advertised or for any opinion expressed herein. **POSTMASTER: Send address changes to Test & Measurement World, P.O. Box 47461, Plymouth, MN 55447. Canada Post: Publications Mail Agreement 40612608. Return undeliverable Canadian addresses to: BleuChip International, P.O. Box 25542, London, ON N6C 6B2.** Printed in U.S.A.

american business media

BPA WORLDWIDE

ADVERTISER INDEX

ADVERTISER	PAGE
Agilent Technologies	C2
Agilent Technologies	7
Agilent Technologies	10
Agilent Technologies	29
Agilent Technologies	43
Agilent Technologies	C3
Ametek Programmable Power	44
AR Worldwide	31
Associated Research	21
Data Translation	35
Geotest	23
IXYS Colorado	37
MathWorks	4
Measurement Computing	40
National Instruments	C4
Newport	6
Omega Engineering	3
Omicron	13
Pickering Interfaces	39
Richardson RFPD	8
Rigol Technologies	27
TDK-Lambda Americas	42
VTI Instruments	19

VIEWPOINT

[An exclusive commentary from a technical leader]

Deterministic jitter and receiver testing

RANSOM STEPHENS
Contributing Editor

Ransom Stephens, PhD, has been confused with Dr. J, not because of any basketball prowess (it always bounces off the rim) but because of his crazy obsession with jitter and equalization and, soon, crosstalk. Yes, he is the novelist and beer-drinking, cussing, Raiders fan of the same name.

Ransom Stephens is the author of the "Eye on Standards" blog on www.tmworld.com. He writes more on the topic of receiver test in "Receiver tolerance testing—with crosstalk!" at bit.ly/HCoho4.

The idea behind receiver tolerance testing is to submit the receiver to "the worst-case but compliant" stress. If it can operate under those conditions, the thinking goes, then it can *inter*operate with any compliant transmitter and channel combination.

Standard applied stresses include some or all of these: a stress-inducing pattern, worst-case rise times and fall times, transmitter de-emphasis, spread-spectrum clocking, interference, random noise, interference or crosstalk emulation, RJ (random jitter), and some combination of DJ (deterministic jitter) or BHPJ (bounded high-probability jitter). Most standards require DJ in a combination of sinusoidal jitter and ISI (intersymbol interference).

SJ (sinusoidal jitter) should be the easiest type of jitter to accurately apply. It is sinusoidal phase modulation. Many pattern generators can apply SJ, but if yours can't, you can use a simple arbitrary waveform generator and modulate the pattern generator's reference clock.

SJ testing usually requires two steps. First, you must apply SJ at a frequency below the clock recovery bandwidth and with amplitude up to and sometimes exceeding a UI (unit interval). Second, you must apply SJ at a frequency beyond the clock-recovery bandwidth and at a substantially lower amplitude. The idea behind the tests is to stress the clock-recovery circuit in a way that ensures that it can roll with the low-frequency punches as well as tolerate reasonable levels of higher-frequency interference.

It is also worthwhile to perform a few tests at frequencies that span the clock-recovery rolloff. The idea is to map the clock-recovery frequency response. Industry specifications don't require such tests, but performing them is a good way to familiarize yourself with the part. While good-old PLLs (phase-locked loops) should respond predictably, some interpolating technologies can have weird resonant effects around the interpolating frequency boundaries near the rolloff.

ISI is caused by the frequency and attenuation response of the channel. It's called ISI because different data sequences have different frequency spectra.

For example, a long string of identical bits has a lot of low-frequency subharmonic content, whereas strings of frequently alternating 1's and 0's are dominated by integer multiples of the fundamental. Because of the unique spectra, the shape of the waveform during different transitions depends on the values of nearby symbols: inter*symbol* interference.

ISI also falls into the categories of "data-dependent jitter" and "correlated jitter," since it's correlated to the data. Keep in mind that ISI is voltage noise, not phase noise, but since the different trajectories cross the voltage slice threshold at different times, ISI causes jitter.

The specifications require prescribed levels of ISI in terms of a calibrated backplane or an S-parameter template. Sometimes, the specification is defined as an equivalent length of trace on standard FR-4 (fire-retardant type-4) media. Some specs (such as DisplayPort) simply require a minimum peak-to-peak ISI jitter level measured in unit intervals; for these cases, you might as well use a simple low-pass filter to apply ISI. While circuits have arbitrarily complicated frequency response, their most obvious overall character is low pass.

The prescription of SJ and ISI imposes horizontal and vertical eye closure that tests several aspects of the receiver. The two SJ tests probe the clock-recovery circuit's frequency response, and the combination of vertical and horizontal eye closure confirms that the decision circuit, including any equalizer, is sufficiently sensitive for the system to perform at the maximum tolerable bit error ratio, usually 10^{-12}. T&MW

To read past Viewpoint columns, go to www.tmworld.com/viewpoint.